SERVO Registers

(**B**ase **A**ddress Refers to the Register of index D3h-D0h, IDSEL = AD18/SB of PCI Configuration Register)

IO Address	Register Name
BA + 00h	SERVO Interrupt Mask Register
BA + 04h	SERVO Interrupt Status Register
BA + 08h	SERVO Sync Register
BA + 0Ch	SERVO[0] Pulse Low Count Register
BA + 10h	SERVO[0] Pulse High Count Register
BA + 14h	SERVO[0] Control Register
BA + 18h	SERVO[1] Pulse Low Count Register
BA + 1Ch	SERVO[1] Pulse High Count Register
BA + 20h	SERVO[1] Control Register
BA + 24h	SERVO[2] Pulse Low Count Register
BA + 28h	SERVO[2] Pulse High Count Register
BA + 2Ch	SERVO[2] Control Register
BA + 30h	SERVO[3] Pulse Low Count Register
BA + 34h	SERVO[3] Pulse High Count Register
BA + 38h	SERVO[3] Control Register
BA + 3Ch	SERVO[4] Pulse Low Count Register
BA + 40h	SERVO[4] Pulse High Count Register
BA + 44h	SERVO[4] Control Register
BA + 48h	SERVO[5] Pulse Low Count Register
BA + 4Ch	SERVO[5] Pulse High Count Register
BA + 50h	SERVO[5] Control Register
BA + 54h	SERVO[6] Pulse Low Count Register

IO Address	Register Name
BA + 58h	SERVO[6] Pulse High Count Register
BA + 5Ch	SERVO[6] Control Register
BA + 60h	SERVO[7] Pulse Low Count Register
BA + 64h	SERVO[7] Pulse High Count Register
BA + 68h	SERVO[7] Control Register
BA + 6Ch	SERVO[8] Pulse Low Count Register
BA + 70h	SERVO[8] Pulse High Count Register
BA + 74h	SERVO[8] Control Register
BA + 78h	SERVO[9] Pulse Low Count Register
BA + 7Ch	SERVO[9] Pulse High Count Register
BA + 80h	SERVO[9] Control Register
BA + 84h	SERVO[10] Pulse Low Count Register
BA + 88h	SERVO[10] Pulse High Count Register
BA + 8Ch	SERVO[10] Control Register
BA + 90h	SERVO[11] Pulse Low Count Register
BA + 94h	SERVO[11] Pulse High Count Register
BA + 98h	SERVO[11] Control Register
BA + 9Ch	SERVO[12] Pulse Low Count Register
BA + A0h	SERVO[12] Pulse High Count Register
BA + A4h	SERVO[12] Control Register
BA + A8h	SERVO[13] Pulse Low Count Register
BA + Ach	SERVO[13] Pulse High Count Register
BA + B0h	SERVO[13] Control Register
BA + B4h	SERVO[14] Pulse Low Count Register

IO Address	Register Name
BA + B8h	SERVO[14] Pulse High Count Register
BA + BCh	SERVO[14] Control Register
BA + C0h	SERVO[15] Pulse Low Count Register
BA + C4h	SERVO[15] Pulse High Count Register
BA + C8h	SERVO[15] Control Register
BA + CCh	SERVO[16] Pulse Low Count Register
BA + D0h	SERVO[16] Pulse High Count Register
BA + D4h	SERVO[16] Control Register
BA + D8h	SERVO[17] Pulse Low Count Register
BA + DCh	SERVO[17] Pulse High Count Register
BA + E0h	SERVO[17] Control Register
BA + E4h	SERVO[18] Pulse Low Count Register
BA + E8h	SERVO[18] Pulse High Count Register
BA + Ech	SERVO[18] Control Register
BA + F0h	SERVO[19] Pulse Low Count Register
BA + F4h	SERVO[19] Pulse High Count Register
BA + F8h	SERVO[19] Control Register
BA + FCh	SERVO[20] Pulse Low Count Register
BA + 100h	SERVO[20] Pulse High Count Register
BA + 104h	SERVO[20] Control Register
BA + 108h	SERVO[21] Pulse Low Count Register
BA + 10Ch	SERVO[21] Pulse High Count Register
BA + 110h	SERVO[21] Control Register
BA + 114h	SERVO[22] Pulse Low Count Register

IO Address	Register Name
BA + 118h	SERVO[22] Pulse High Count Register
BA + 11Ch	SERVO[22] Control Register
BA + 120h	SERVO[23] Pulse Low Count Register
BA + 124h	SERVO[23] Pulse High Count Register
BA + 128h	SERVO[23] Control Register
BA + 12Ch	SERVO[24] Pulse Low Count Register
BA + 130h	SERVO[24] Pulse High Count Register
BA + 134h	SERVO[24] Control Register
BA + 138h	SERVO[25] Pulse Low Count Register
BA + 13Ch	SERVO[25] Pulse High Count Register
BA + 140h	SERVO[25] Control Register
BA + 144h	SERVO[26] Pulse Low Count Register
BA + 148h	SERVO[26] Pulse High Count Register
BA + 14Ch	SERVO[26] Control Register
BA + 150h	SERVO[27] Pulse Low Count Register
BA + 154h	SERVO[27] Pulse High Count Register
BA + 158h	SERVO[27] Control Register
BA + 15Ch	SERVO[28] Pulse Low Count Register
BA + 160h	SERVO[28] Pulse High Count Register
BA + 164h	SERVO[28] Control Register
BA + 168h	SERVO[29] Pulse Low Count Register
BA + 16Ch	SERVO[29] Pulse High Count Register
BA + 170h	SERVO[29] Control Register
BA + 174h	SERVO[30] Pulse Low Count Register

IO Address	Register Name
BA + 178h	SERVO[30] Pulse High Count Register
BA + 17Ch	SERVO[30] Control Register
BA + 180h	SERVO[31] Pulse Low Count Register
BA + 184h	SERVO[31] Pulse High Count Register
BA + 188h	SERVO[31] Control Register

SERVO Registers

I/O Port: BA + 00h

Register Name: SERVO Interrupt Mask Register

Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIM[31-0]																															

Bit	Name	Attribute	Description
31-0	SIM[31-0]	R/W	SERVO[31-0] Interrupt Mask Register 1: Enable Interrupt 0: Disable Interrupt

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I/O Port: BA + 04h

Register Name: SERVO Interrupt Status Register

Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIS[31-0]																															

Bit	Name	Attribute	Description
31-0	SIS[31-0]	R/W	SERVO[31-0] Interrupt Status Register 1: Interrupt happen and write “1” to clear 0: No Interrupt

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I/O Port: BA + 08h

Register Name: SERVO Sync Status Register

Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC[31-0]																															

Bit	Name	Attribute	Description
31-0	SYNC[31-0]	R/W	SERVO[31-0] Sync Register 1: SERVO will be hold 0: SERVO without hold

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I/O Port: BA + 0Ch, 18h, 24h, 30h, 3Ch, 48h, 54h, 60h, 6Ch, 78h, 84h, 90h, 9Ch, A8h, B4h, C0h,

CCh, D8h, E4h, F0h, FCh,108h,114h,120h,12Ch,138h,144h,150h,15Ch,168h,174h,180h

Register Name: SERVO Pulse Low Register

Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPL																															

Bit	Name	Attribute	Description
31-0	SPL	R/W	SERVO Pulse Low Register. SERVO clock is 10MHz

I/O Port: BA + 10h, 1Ch, 28h, 34h, 40h, 4Ch, 58h, 64h, 70h, 7Ch, 88h, 94h, A0h, Ach, B8h, C4h, D0h, DCh, E8h, F4h,100h,10Ch,118h,124h,130h,13Ch,148h,154h,160h,16Ch,178h,184h

Register Name: SERVO Pulse High Register

Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPH																															

Bit	Name	Attribute	Description
31-0	SPH	R/W	SERVO Pulse High Register. SERVO clock is 10MHz

I/O Port: BA + 14h, 20h, 2Ch, 38h, 44h, 50h, 5Ch, 68h, 74h, 80h, 8Ch, 98h, A4h, B0h, BCh, C8h, D4h, E0h, Ech, F8h,104h,110h,11Ch,128h,134h,140h,14Ch,158h,164h,170h,17Ch,188h

Register Name: SERVO Control Register

Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SE	CM	INVS	Rsvd	RC																											

Bit	Name	Attribute	Description
31	SE	R/W	SERVOx Enable Control 1: SERVOx enable 0: SERVOx disable
30	CM	R/W	SERVOx Continuous Mode 1: SERVOx Continuous Mode enable 0: SERVOx Continuous Mode disable
29	INVS	R/W	Inverse SERVO signal 0: default SERVO out ‘0’, SPH specify ‘I’, SPL specify “0”. 1: Inverse output signal of upper case
28	Rsvd	RO	Reserved
27-0	RC	R/W	SERVOx Repeat Count. It is used when CM=0.

SB Configuration Space Registers (IDSEL = AD18/Device 7)

Register Offset: CBh – C8h

Register Name: Internal Peripheral Feature Control Register II

Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GS[31-24]								GS[23-16]								GS[15-8]								GS[7-0]							

Bit	Name	**Attribute**	Description
31-24	GS[31-24]	R/W	GPIO_P4[7-0] and SERVO[31-24] selection. This register is used only when SB register C0h bit1 is “1”. 0: PINS for GPIO_P4 (default) 1: PINS for SERVO
23 – 16	GS[23-16]	R/W	GPIO_P2[7-0] and SERVO[23-16] selection. This register is used only when STRAP[1] (NB register 60h bit19) is “1”. 0: PINS for GPIO_P2 (default) 1: PINS for SERVO
15 – 8	GS[15-8]	R/W	GPIO_P1[7-0] and SERVO[15-8] selection. 0: PINS for GPIO_P1 (default) 1: PINS for SERVO
7 – 0	GS[7-0]	R/W	GPIO_P0[7-0] and SERVO[7-0] selection. 0: PINS for GPIO_P0 (default) 1: PINS for SERVO

Register Offset: D3h – D0h

Register Name: Internal SERVO Control Register

Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Reserved	CLKS	UE	Rsvd	SIRT	UIOA	Reserved

Bit	Name	**Attribute**	Description
31-25	Rsvd	RO	Reserved
24	CLKS	R/W	Servo Clock selection 0: 10MHz (default) 1: 50MHz
23	UE	R/W	Enable/Disable Internal SERVO IO Address Decode 0: Disable (Default) 1: Enable
22-20	Rsvd	RO	Reserved
19-16	SIRT	R/W	SERVO IRQ Routing Table Bit19 Bit18 Bit17 Bit16 Routing Table 0 0 0 0 Disable. 0 0 0 1 IRQ[9] 0 0 1 0 IRQ[3] 0 0 1 1 IRQ[10] 0 1 0 0 IRQ[4] 0 1 0 1 IRQ[5] 0 1 1 0 IRQ[7] 0 1 1 1 IRQ[6] 1 0 0 0 IRQ[1] 1 0 0 1 IRQ[11] 1 0 1 0 Reserved 1 0 1 1 IRQ[12] 1 1 0 0 Reserved 1 1 0 1 IRQ[14] 1 1 1 0 Reserved 1 1 1 1 IRQ[15] These four bits are used to route SERVO IRQ to any 8259 Interrupt lines. The BIOS should be

Bit	Name	Attribute	Description
			used to inhibit the setting of the reserved value.
15-9	UIOA	R/W	Internal SERVO IO Address. The Bit[15:9] contain the base IO address A[15:9] of internal SERVO.
8-0	Rsvd	RO	Reserved. All are ‘0’s. Writing any value to these bits causes no effect.