iC-NQC

preliminary

13-bit Sin/D CONVERTER WITH SIGNAL CALIBRATION

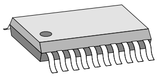
FEATURES

- Resolution of up to 8,192 angle steps per sine period
- Binary and decimal resolution settings, e.g. 500, 512, 1000, 1024; programmable angle hysteresis
- Count-safe vector follower principle, real-time system with 70 MHz sampling rate
- Conversion time of just 250 ns including amplifier settling
- Direct sensor connection; selectable input gain
- Input frequency of up to 250 kHz
- Signal conditioning for offset, amplitude and phase
- A/B quadrature signals of up to 3.75 MHz with adjustable minimum transition distance
- Zero signal processing, adjustable in index position and width
- Absolute angle output via fast serial interface (BiSS, SSI)
- Permanent bidirectional memory access to parameters and OEM data by BiSS C
- Period counting with up to 24 bits
- Error monitoring of frequency, amplitude and configuration
- Device setup from serial EEPROM or using BiSS
- ESD protection and TTL-/CMOS-compatible outputs

APPLICATIONS

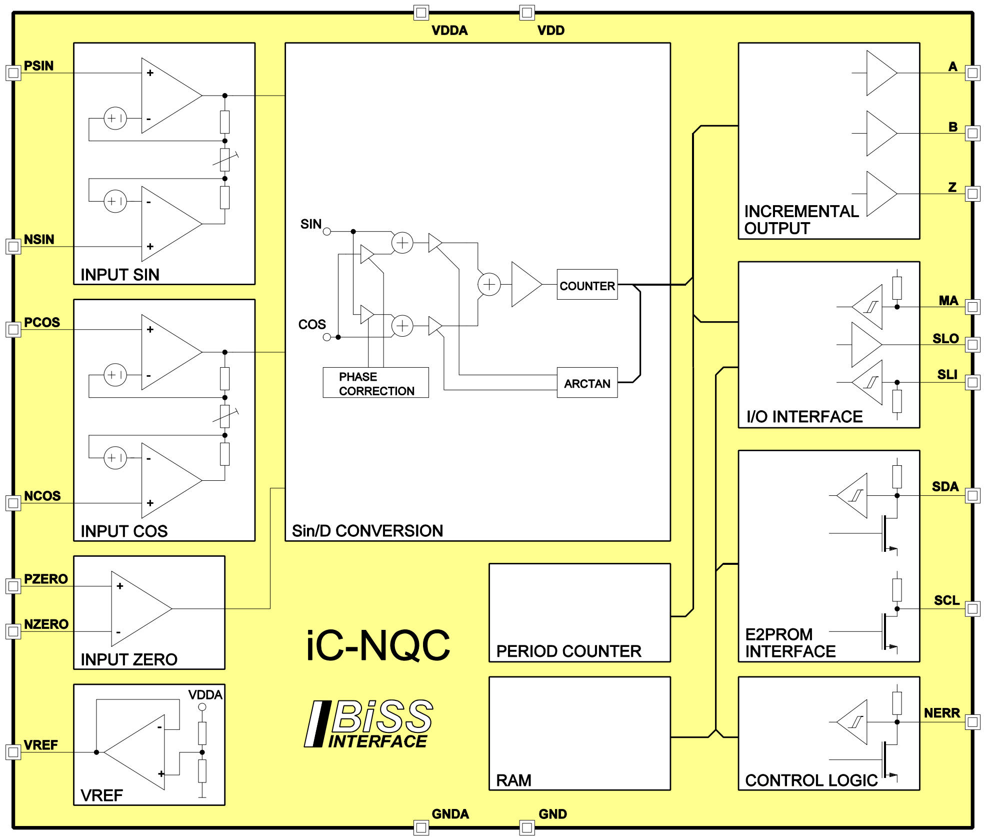
- Interpolator IC for angle resolution from sine/cosine sensor signals
- Optical encoders
- MR sensor systems

PACKAGES



TSSOP20

BLOCK DIAGRAM



DESCRIPTION

iC-NQC is a monolithic A/D converter which, by applying a count-safe vector follower principle, converts sine/cosine sensor signals with a selectable resolution and hysteresis into angle position data.

This absolute value is output via a bidirectional, synchronous-serial I/O interface in BiSS C protocol and trails a master clock rate of up to 10 Mbit/s. Alternatively, this value can be output so that it is compatible with SSI in Gray or binary code, with or without error bits. The device also supports double transmission in SSI ring mode.

Signal periods are logged quickly by a 24-bit period counter that can supplement the output data with an upstream multiturn position value.

At the same time any changes in angle are converted into incremental A QUAD B signals. Here, the minimum transition distance can be stipulated and adapted to suit the system on hand (cable length, external counter). A synchronized zero index Z is generated if enabled by PZERO and NZERO.

The front-end amplifiers are configured as instrumentation amplifiers, permitting sensor bridges to be directly connected without the need for external resistors. Various programmable D/A converters are available for the conditioning of sine/cosine sensor signals with regard to offset, amplitude ratio and phase errors (offset compensation by 8-bit DAC, gain ratio by 5-bit DAC, phase compensation by 6-bit DAC).

The front-end gain can be set in stages graded to suit all common complementary sensor signals from approximately 20 mVpp to 1.5 Vpp and also non-complementary sensor signals from 40 mVpp to 3 Vpp respectively.

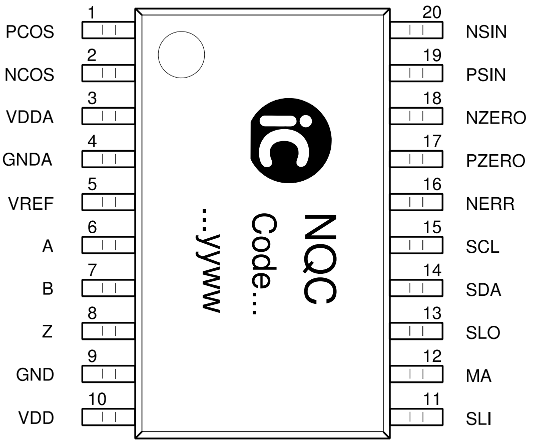
The device can be configured using two bidirectional interfaces, the EEPROM interface from a serial EEPROM with I^2C interface, or the I/O interface in BiSS C protocol. Free storage space on the EEPROM can be accessed via BiSS for the storage of additional data.

After a low voltage reset, iC-NQC reads in the configuration data including the check sum (CRC) from the EEPROM and repeats the process if a CRC error is detected.

CONTENTS

PACKAGES TSSOP20 (according to JEDEC Standard)

PIN CONFIGURATION
TSSOP20 4.4 mm, lead pitch 0.65 mm



PIN FUNCTIONS

No.	Name	Function
1	PCOS	Input Cosine +
2	NCOS	Input Cosine -
3	VDDA	+5 V Supply Voltage (analog)
4	GNDA	Ground (analog)
5	VREF	Reference Voltage Output
6	A	Incremental Output A Analog signal COS+ (TMA mode) PWM signal for Offset Sine (calib.)
7	B	Incremental Output B Analog signal COS- (TMA mode) PWM signal for Offset Cosine (calib.)
8	Z	Incremental Output Z PWM signal for Phase/Ratio (calib.)
9	GND	Ground
10	VDD	+5 V Supply Voltage (digital)
11	SLI	I/O Interface, data input*
12	MA	I/O Interface, clock line
13	SLO	I/O Interface, data output
14	SDA	EEPROM interface, data line Analog signal SIN+ (TMA mode)
15	SCL	EEPROM interface, clock line Analog signal SIN- (TMA mode)
16	NERR	Error Input/Output, active low
17	PZERO	Input Zero Signal +
18	NZERO	Input Zero Signal -
19	PSIN	Input Sine +
20	NSIN	Input Sine -

External connections linking VDDA to VDD and GND to GNDA are required.
*) If only a single iC-NQC is used and no chain circuitry of multiple BiSS slaves, pin SLI can remain unwired or can be linked to ground (GND).

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply permissible operating conditions; functional operation is not guaranteed.
Exceeding these ratings may damage the device.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDDA	Voltage at VDDA		-0.3	6	V
G002	VDD	Voltage at VDD		-0.3	6	V
G003	Vpin()	Voltage at PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF, NERR, SCL, SDA, MA, SLI, SLO, A, B, Z	V() < VDDA + 0.3 V V() < VDD + 0.3 V	-0.3	6	V
G004	Imx(VDDA)	Current in VDDA		-50	50	mA
G005	Imx(GNDA)	Current in GNDA		-50	50	mA
G006	Imx(VDD)	Current in VDD		-50	50	mA
G007	Imx(GND)	Current in GND		-50	50	mA
G008	Imx()	Current in PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF, NERR, SCL, SDA, MA, SLI, SLO, A, B, Z		-10	10	mA
G009	Ilu()	Pulse Current in all pins (Latch-up Strength)	according to Jedec Standard No. 78; Ta = 25 °C, pulse duration to 10 ms, VDDA = $VDDA_{max}$, VDD = VDD_{max}, Vlu() = (-0.5...+1.5) x $Vpin()_{max}$	-100	100	mA
G010	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G011	Tj	Junction Temperature		-40	150	°C
G012	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating Conditions: VDDA = VDD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended temperature range of -40 to 125 °C available on request)		-25		85	°C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA = VDD = 5 V ±10 %, Tj = -40 ... 125 °C, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device Functionality and parameters beyond the operating conditions (with reference to independent voltage supplies, for instance) are to be verified within the individual application using FMEA methods.							
001	VDDA, VDD	Permissible Supply Voltage		4.5		5.5	V
002	I(VDDA)	Supply Current in VDDA	fin() = 200 kHz; A, B, Z open			15	mA
003	I(VDD)	Supply Current in VDD	fin() = 200 kHz; A, B, Z open			20	mA
004	Von	Turn-on Threshold VDDA, VDD		3.2		4.4	V
005	Vhys	Turn-on Threshold Hysteresis		200			mV
006	Vc()hi	Clamp Voltage hi at PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF	Vc()hi = V() - VDDA; I() = 1 mA, other pins open	0.3		1.6	V
007	Vc()lo	Clamp Voltage lo at PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF, NERR, SCL, SDA, MA, SLI, SLO, A, B, Z	I() = -1 mA, other pins open	-1.6		-0.3	V
008	Vc()hi	Clamp Voltage hi at NERR, SCL, SDA, MA, SLI, SLO, A, B, Z	Vc()hi = V() - VDD; I() = 1 mA, other pins open	0.3		1.6	V
Input Amplifiers and Signal Inputs PSIN, NSIN, PCOS, NCOS							
101	Vos()	Input Offset Voltage	Vin() and G() in accordance with table GAIN; G ≥ 20 G < 20	 -10 -15		 10 15	 mV mV
102	TCos	Input Offset Voltage Temperature Drift	see 101		±10		µV/K
103	Iin()	Input Current	V() = 0 V ... VDDA	-50		50	nA
104	GA	Gain Accuracy	G() in accordance with table GAIN	95		102	%
105	GArel	Gain SIN/COS Ratio Accuracy	G() in accordance with table GAIN	97		103	%
106	fhc	Cut-off Frequency	G = 80 G = 2.667	150 630			kHz kHz
107	SR	Slew Rate	G = 80 G = 2.667	2.3 8.0			V/µs V/µs
Sine-To-Digital Conversion							
201	AAabs	Absolute Angle Accuracy without calibration	referred to 360° input signal, G = 2.667, Vin = 1.5 Vpp, HYS = 0	-1.0		1.0	DEG
202	AAabs	Absolute Angle Accuracy after calibration	referred to 360° input signal, HYS = 0, internal signal amplitude of 2 ... 4 Vpp	-0.5	±0.35	+0.5	DEG
203	AArel	Relative Angle Accuracy	referred to signal periods at A, resp. B (see Fig. 1); G = 2.667, Vin = 1.5 Vpp, SELRES = 1024, FCTR = 0x0004 ... 0x00FF, fin < fin_{max} (see table 15)	-10		10	%
Reference Voltage Output VREF							
801	VREF	Reference Voltage	I(VREF) = -1 mA ... +1 mA	48		52	% VDDA
Oscillator							
A02	fosc()	Oscillator Frequency	presented at pin SCL with subdivision of 2048; VDDA = VDD = 5 V ±10 % VDDA = VDD = 5 V	 56 60	 74	 90 86	 MHz MHz
A03	TCosc	Oscillator Frequency Temperature Drift	VDDA = VDD = 5 V		-0.1		%/K
A04	VCosc	Oscillator Frequency Power Supply Dependance			+9		%/V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA = VDD = 5 V ±10 %, Tj = -40 ... 125 °C, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Zero Signal Enable Inputs PZERO, NZERO							
B01	Vos()	Input Offset Voltage	V() = Vcm()	-20		20	mV
B02	Iin()	Input Current	V() = 0 V ... VDDA	-50		50	nA
B03	Vcm()	Common-Mode Input Voltage Range		1.4		VDDA-1.5	V
B04	Vdm()	Differential Input Voltage Range		0		VDDA	V
Incremental Outputs A, B, Z and I/O Interface Output SLO							
D01	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); I() = -4 mA			0.4	V
D02	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.4	V
D03	tr()	Rise Time	CL() = 50 pF			60	ns
D04	tf()	Fall Time	CL() = 50 pF			60	ns
D05	RL()	Permissible Load at A, B	TMA = 1 (calibration mode)	1			MΩ
I/O Interface Inputs MA, SLI							
E01	Vt()hi	Threshold Voltage hi				2	V
E02	Vt()lo	Threshold Voltage lo		0.8			V
E03	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	300			mV
E04	Ipu(MA)	Pull-up Current in MA	V() = 0 ... VDD - 1 V	-240	-120	-25	µA
E05	Ipd(SLI)	Pull-down Current in SLI	V() = 1 ... VDD	20	120	300	µA
E06	fclk(MA)	Permissible MA Clock Frequency	SSI protocol BiSS protocol			4 10	MHz MHz
E07	tp(MA-SLO)	Propagation Delay: MA edge vs. SLO output	RL(SLO) $\geq$ 1 kΩ	10		50	ns
E08	tbusy_s	Processing Time Single-Cycle Data (delay of start bit)			0		µs
E09	tbusy_r	Processing Time Register Access (delay of start bit)	with read access to EEPROM			2	ms
E10	tidle	Interface Blocking Time	powering up with no EEPROM		1	1.5	ms
E11	t_tos	Timeout	TIMO = 0, TOA =0		20		µs
EEPROM Interface Inputs SDA and Error Input NERR							
F01	Vt()hi	Threshold Voltage hi				2	V
F02	Vt()lo	Threshold Voltage lo		0.8			V
F03	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	300			mV
F04	tbusy()cfg	Duration of Startup Configuration	error free EEPROM access		5	7	ms
EEPROM Interface Outputs SDA, SCL and Error Output NERR							
G01	f()	Write/Read Clock at SCL			20	100	kHz
G02	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.45	V
G03	Ipu()	Pull-up Current	V() = 0 ... VDD - 1 V	-600	-300	-75	µA
G04	ft()	Fall Time	CL() = 50 pF			60	ns
G05	tmin()lo	Min. Duration Of Error Indication at NERR (lo signal)	MA = hi, no BiSS access, amplitude or frequeny error	10			ms
G06	Tpwm()	Cycle Duration Of Error Indication at NERR	fosc() subdivided 2^{22}		60.7		ms
G07	t()lo	Duty Cycle Of Error Indication at NERR	signal duration low to high; AERR = 0 (amplitude error) FERR = 0 (frequency error)		 75 50		 % %
G08	RL()	Permissible Load at SDA, SCL	TMA = 1 (calibration mode)	1			MΩ

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA = VDD = 5 V ±10 %, Tj = -40 ... 125 °C, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Signal Monitoring							
H01	Vth	Voltage Threshold for Monitoring of Minimal Amplitude	VDDA = 5 V, SELAMPL = 0, AMPL = 0x00, PHI: 0°, 90°, 180°, 270° AMPL = 0x01, PHI: 0° AMPL = 0x02, PHI: 0° AMPL = 0x03, PHI: 0°	 2.8 3.0 3.2 3.4	 3.0 3.2 3.4 3.6	 3.2 3.4 3.6 3.8	 V V V V
H02	Vthmax	Upper Voltage Threshold for Monitoring of Sin^2+Cos^2	VDDA = 5 V, SELAMPL = 1, AMPL = 0x04...0x07, PHI: 0°, 45°...315°	 3.35	 4.5	 4.85	 V
H03	Vthmin	Lower Voltage Threshold for Monitoring of Sin^2+Cos^2	VDDA = 5 V, SELAMPL = 1, AMPL = 0x04, PHI: 0°, 45°...315° AMPL = 0x05, PHI: 45° AMPL = 0x06, PHI: 45° AMPL = 0x07, PHI: 45°	 0.2 0.6 1.1 1.6	 1.0 1.5 2.0 2.5	 1.5 2.0 2.5 3.0	 V V V V

CHARACTERISTICS: Diagrams

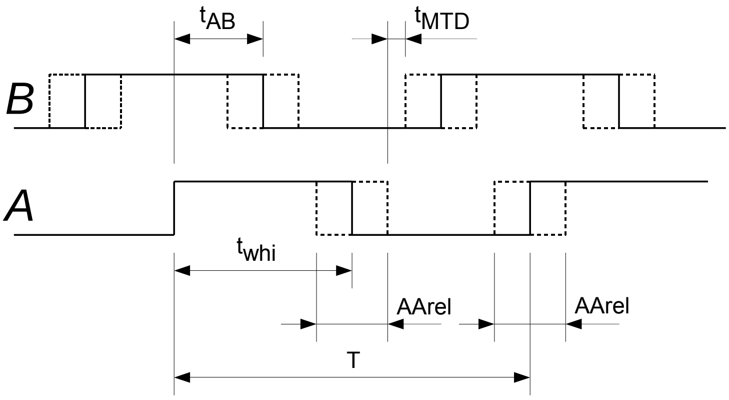


Figure 1: Definition of relative angle error and minimum transition distance

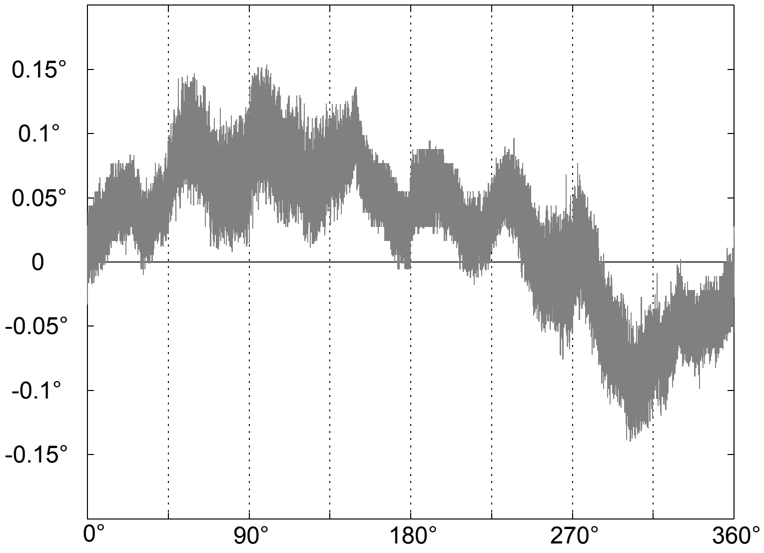


Figure 2: Typical residual absolute angle error after calibration.

OPERATING REQUIREMENTS: I/O Interface

Operating Conditions: VDD = 5 V ±10 %, Ta = -25 ... 85 °C; input levels lo = 0 ... 0.45 V, hi = 2.4 V ... VDD

Item No.	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
SSI Protocol							
I001	T_{MAS}	Permissible Clock Period	t_{tos} according to Table 44	4	250	2x t_{tos}	ns
I002	t_{MASh}	Clock Signal Hi Level Duration		4	25	t_{tos}	ns
I003	t_{MASl}	Clock Signal Lo Level Duration		4	25	t_{tos}	ns
BiSS C Protocol							
I004	T_{MAS}	Permissible Clock Period	t_{tos} according to Table 34	5	100	2x t_{tos}	ns
I005	t_{MASh}	Clock Signal Hi Level Duration		5	25	t_{tos}	ns
I006	t_{MASl}	Clock Signal Lo Level Duration		5	25	t_{tos}	ns

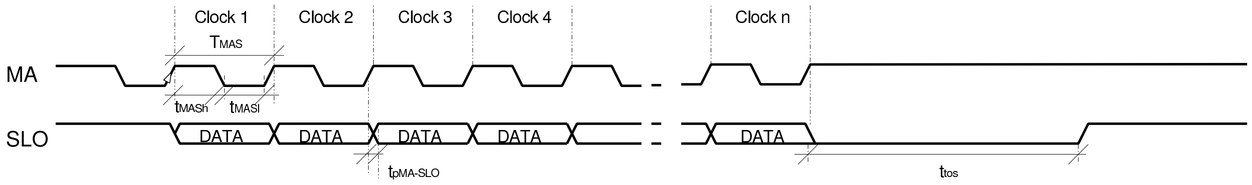


Figure 3: Timing diagram in SSI protocol.

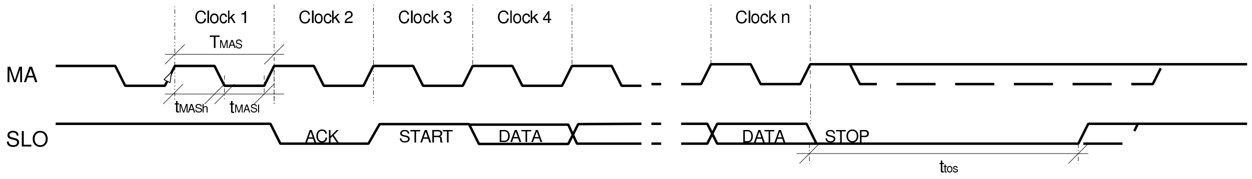


Figure 4: Timing diagram in BiSS C protocol.

PARAMETER and REGISTER

Register Description, Overview .... Page 10

Signal Conditioning .... Page 11

GAIN:	Gain Select
SINOFFS:	Offset Calibration Sine
COSOFFS:	Offset Calibration Cosine
REFOFFS:	Offset Calibration Reference
RATIO:	Amplitude Calibration
PHASE:	Phase Calibration

Converter Function .... Page 12

SELRES:	Resolution
HYS:	Hysteresis
FCTR:	Max. Permissible Converter Frequency

Incremental Signals .... Page 15

CFGABZ:	Output A, B, Z
ROT:	Direction of Rotation
CBZ:	24-bit Period Counter Configuration
ENRESDEL:	Output Delay A, B, Z
ZPOS:	Zero Signal Position
CFGZ:	Zero Signal Length
CFGAB:	Zero Signal Logic

Signal Monitoring and Error Messages .... Page 17

SELAMPL:	Amplitude Monitoring, function
AMPL:	Amplitude Monitoring, thresholds
AERR:	Amplitude Error
FERR:	Frequency Error

Test Functions .... Page 18

TMODE:	Test Mode
TMA:	Analog Test Mode

BiSS Interface .... Page 19

SELSSI:	Protocol Version
TIMO, TOA:	Timeout
TOS:	Timeout Short**
M2S:	Data Output and Options
CRC6:	CRC Polynomial
NZB:	Zero Bit
ENCDS:	Protocol Options
RPL:	Register Protection Settings
GRAY:	SSI Data Format

OVERVIEW

Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	ENCDS	M2S(1:0)		SELRES(4:0)				
0x01	HYS(2:0)			ZPOS(4:0)				
0x02	ENRESDEL	SELSSI	ROT	CBZ	CFGABZ(1:0)		CFGZ(1:0)	
0x03	CRC6	NZB	CFGAB(1:0)		RPL	0	AERR	FERR
0x04	FCTR(7:0)							
0x05	GRAY	FCTR(14:8)						
0x06	reserved*		TIMO	0	TMODE(2:0)			TMA
0x07	reserved*				TOA	reserved*		
0x08	GAIN(3:0)				RATIO(3:0)			
0x09	SINOFFS(7:0)							
0x0A	COSOFFS(7:0)							
0x0B	PHASE(5:0)						REFOFFS	RATIO(4)
0x0C	reserved*					SELAMPL	AMPL(1:0)	
0x0D								
0x0E								
0x0F	CRC_E2P(7:0) - check value read from the EEPROM for addresses 0x00 to 0x0E							
	EEPROM							
0x10 - 0x1F	0x00 - 0x0F	Reserved EEPROM memory section: iC-NQC device configuration data.						
0x41 - 0x7F	0x31 - 0x6F	Reserved EEPROM memory section: BiSS C Slave Registers (device identifier 4E 51 43 35 00 00 69 43)						

Register contents are random when powering up without an EEPROM.

When no register protection is active, all registers permit read and write access (see RPL).

*) Reserved registers must be programmed to zero. **) For TOS see table 42 on page 21.

Table 5: Register layout

SIGNAL CONDITIONING

Input stages SIN and COS are configured as instrumentation amplifiers. The amplifier gain must be selected in accordance with the input signal amplitude and programmed to register GAIN according to the following table. Half of the supply voltage is available at VREF as a center voltage to enable the DC level to be adapted.

GAIN	Adr 0x08, Bit 7:4				
		Sine/Cosine Input Signal Levels Vin()			
		Amplitude		Average value (DC)	
Code	Amplification	Differential	Single-ended	Differential	Single-ended
0x0F	80.000	up to 50 mVpp	up to 100 mVpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.2 V
0x0E	66.667	up to 60 mVpp	up to 120 mVpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.2 V
0x0D	53.333	up to 75 mVpp	up to 0.15 Vpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.2 V
0x0C	40.000	up to 0.1 Vpp	up to 0.2 Vpp	1.2 V ... VDDA - 1.2 V	1.3 V ... VDDA - 1.3 V
0x0B	33.333	up to 0.12 Vpp	up to 0.24 Vpp	1.2 V ... VDDA - 1.2 V	1.3 V ... VDDA - 1.3 V
0x0A	28.571	up to 0.14 Vpp	up to 0.28 Vpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.3 V
0x09	26.667	up to 0.15 Vpp	up to 0.3 Vpp	1.2 V ... VDDA - 1.2 V	1.3 V ... VDDA - 1.3 V
0x08	20.000	up to 0.2 Vpp	up to 0.4 Vpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.3 V
0x07	14.287	up to 0.28 Vpp	up to 0.56 Vpp	1.2 V ... VDDA - 1.3 V	1.4 V ... VDDA - 1.4 V
0x06	10.000	up to 0.4 Vpp	up to 0.8 Vpp	1.2 V ... VDDA - 1.3 V	1.4 V ... VDDA - 1.5 V
0x05	8.000	up to 0.5 Vpp	up to 1 Vpp	0.8 V ... VDDA - 1.4 V	1.0 V ... VDDA - 1.6 V
0x04	6.667	up to 0.6 Vpp	up to 1.2 Vpp	0.8 V ... VDDA - 1.4 V	1.1 V ... VDDA - 1.7 V
0x03	5.333	up to 0.75 Vpp	up to 1.5 Vpp	0.9 V ... VDDA - 1.5 V	1.3 V ... VDDA - 1.9 V
0x02	4.000	up to 1 Vpp	up to 2 Vpp	1.2 V ... VDDA - 1.6 V	1.7 V ... VDDA - 2.1 V
0x01	3.333	up to 1.2 Vpp	up to 2.4 Vpp	1.2 V ... VDDA - 1.7 V	1.8 V ... VDDA - 2.3 V
0x00	2.667	up to 1.5 Vpp	up to 3 Vpp	1.3 V ... VDDA - 1.8 V	2.0 V ... VDDA - 2.6 V

Table 6: Input gain

SINOFFS	Adr 0x09, Bit 7:0	
COSOFFS	Adr 0x0A, Bit 7:0	
Code	Output Offset	Input Offset
0x00	0 V	0 V
0x01	-7.8125 mV	-7.8125* mV / GAIN
...	...	...
0x7F	-0.9922 V	-0.9922 V / GAIN
0x80	0 V	0 V
0x81	+7,8125 mV	+7.8125 mV / GAIN
...	...	...
0xFF	+0.9922 V	+0.9922 V / GAIN
Notes	*) With REFOFFS = 0x00 and VDDA = 5 V.	

Table 7: Sine/cosine offset calibration

REFOFFS	Adr 0x0B, Bit 1
Code	Reference Voltage
0x00	Dependent on VDDA (example of application: MR sensors)
0x01	Not dependent on VDDA (example of application: Sin/Cos encoders)

Table 8: Offset reference

RATIO	Adr 0x0B, Bit 0, Adr 0x08, Bit 3:0		
Code	COS / SIN	Code	COS / SIN
0x00	1.0000	0x10	1.0000
0x01	1.0067	0x11	0.9933
...	...	...	...
0x0F	1.1	0x1F	0.9000

Table 9: Amplitude calibration

PHASE	Adr 0x0B, Bit 7:2		
Code	Phase Shift	Code	Phase Shift
0x00	90°	0x20	90°
0x01	90.703125°	0x21	89.296875°
...	...	...	...
0x12	102.65625°	0x32	77.34375°
...	102.65625°	...	77.34375°
0x1F	102.65625°	0x3F	77.34375°

Table 10: Phase calibration

CONVERTER FUNCTIONS

SELRES	Adr 0x00, Bit 4:0	
Code	Binary Resolutions	Examples of Permissible Input Frequencies fin$_{max}$ (FCTR 0x0004, 0x4302)
0x00	-	
0x01	-	
0x02	-	
0x03	8192	158 Hz, 1.06 kHz
0x04	4096	317 Hz, 2.12 kHz
0x05	2048	634 Hz, 4.24 kHz
0x06	1024	1.27 kHz, 8.5 kHz
0x07	512	2.54 kHz, 17 kHz
0x08	256	5.1 kHz, 34 kHz
0x09	128	10.2 kHz, 68 kHz
0x0A	64	20.3 kHz, 136 kHz
0x0B	32	40.6 kHz (max. 250 kHz)
0x0C	16	81.3 kHz (max. 250 kHz)
0x0D	8	162 kHz (max. 250 kHz)
0x0E	-	
0x0F	-	

Table 11: Binary resolutions

SELRES	Adr 0x00, Bit 4:0	
Code	Decimal Resolutions	Examples of Permissible Input Frequencies fin$_{max}$ (FCTR 0x0004, 0x4302)
0x10	2000	650 Hz, 4.3 kHz
0x11	1600	812 Hz, 5.5 kHz
0x12	1000	1.3 kHz, 8.6 kHz
0x13	800	1.6 kHz, 10.8 kHz
0x14	500	2.6 kHz, 17 kHz
0x15	400	3.2 kHz, 22 kHz
0x16	250 ^{*1}	5.2 kHz, 35 kHz
0x17	125 ^{*1,2}	5.2 kHz, 35 kHz
0x18	320	4.1 kHz, 27 kHz
0x19	160 ^{*2}	4.1 kHz, 27 kHz
0x1A	80 ^{*4}	4.1 kHz, 27 kHz
0x1B	40 ^{*8}	4.1 kHz, 27 kHz
0x1C	200	6.5 kHz, 43.3 kHz
0x1D	100 ^{*2}	6.5 kHz, 43.3 kHz
0x1E	50 ^{*1,4}	6.5 kHz, 43.3 kHz
0x1F	25 ^{*1,8}	6.5 kHz, 43.3 kHz
Notes	^{*1} Not suitable for incremental output on A, B. ^{*2,4,8} The internal resolution is higher by a factor of 2, 4 or 8.	

Table 12: Decimal resolutions

HYS	Adr 0x01, Bit 7:5		
Code	Hysteresis in degrees	Hysteresis in LSB	Absolute error*
0x00	0°		
0x01	0.0879°	1 LSB @ 12 bit	0.044°
0x02	0.1758°	1/2 LSB @ 10 bit	0.088°
0x03	0.3516°	1 LSB @ 10 bit	0.176°
0x04	0.7031°	1/2 LSB @ 8 bit	0.352°
0x05	1.4063°	1 LSB @ 8 bit	0.703°
0x06	5.625°		2.813°
0x07	45°	only recommended for calibration	22.5°
Notes	*) The resulting absolute error is equivalent to half the angle hysteresis.		

Table 13: Hysteresis

MAXIMUM POSSIBLE CONVERTER FREQUENCY

The converter frequency automatically adjusts to the value required by the input frequency and resolution. This value ranges from zero to a maximum dependent on the oscillator frequency that is set via register FCTR.

Serial data output

For BiSS or SSI output the maximum possible converter frequency can be adjusted to suit the maximum input frequency; an automatic converter resolution step-down feature can be enabled via the FCTR register. Should the input frequency exceed the frequency limit of the selected converter resolution, the LSB is kept stable and not resolved any further; the interpolation resolution halves.

If the next frequency limit is overshot, the LSB and LSB +1 are kept stable and so on. If the input frequency again sinks below this frequency threshold, fine resolution automatically returns.

With the programming of CRC6 = 1 a resolution step-down will be signalled via the BiSS warning bit.

Max. Possible Converter Frequency For Serial Data Output

	Resolution Requirements			Protocol		Max. Input Frequency	Restrictions at high input frequency	Examples* fin_{max} [kHz] at resol.		
FCTR	**Min. Res.**	**bin**	**dec**	**BiSS**	**SSI**	**fin_{max}**		**8192**	**1024**	**200**
0x0004		X	X	X	X	fosc()min / 40 / Resolution	–	0.17	1.37	7.0
0x4102	≥ 8	X	X	X	X	fosc()min / 24 / Resolution	Rel. angle error 2x increased	0.28	2.3	11.7
0x4202	≥ 16	X	X	X	X	2 x fosc()min / 24 / Res.	Rel. angle error 4x increased	0.57	4.6	23.3
0x4302	≥ 32	X	X	X	X	4 x fosc()min / 24 / Res.	Rel. angle error 8x increased	1.14	9.1	46.7
0x4702	≥ 64	X	-	X	X	8 x fosc()min / 24 / Res.	Resolution lowered by factor of 2	2.3	18.2	-
0x4B02	≥ 128	X	-	X	X	16 x fosc()min / 24 / Res.	Res. lowered by factor of 2-4	4.6	36.5	-
0x4F02	≥ 256	X	-	X	X	32 x fosc()min / 24 / Res.	Res. lowered by factor of 2-8	9.1	72.9	-
0x5302	≥ 512	X	-	X	X	64 x fosc()min / 24 / Res.	Res. lowered by factor of 2-16	18.2	146	-
0x5702	≥ 1024	X	-	X	X	128 x fosc()min / 24 / Res.	Res. lowered by factor of 2-32	36.5	250	-
0x5B02	≥ 2048	X	-	X	X	256 x fosc()min / 24 / Res.	Res. lowered by factor of 2-64	72.9	-	-
0x5F02	≥ 4096	X	-	X	X	512 x fosc()min / 24 / Res.	Res. lowered by factor of 2-128	146	-	-
0x6302	8192	X	-	X	X	1024 x fosc()min / 24 / Res.	Res. lowered by factor of 2-256	250	-	-
Notes	*) Calculated with fosc()min taken from Electrical Characteristics, item A02.									

Table 14: Maximum converter frequency for serial data output.

Incremental output to A, B and Z

Settings for the maximum possible converter frequency using register FCTR are governed by two criteria:

1. The maximum input frequency
2. System restrictions caused by slow counters or data transmission via cable

In this case it is sensible to preselect a minimum transition distance for the output signals. These settings also make a suitable zero-delay digital glitch filter that acts on ESD impact on the sensor and keeps the output signals spike free through temporal separation, for example.

Serial data output is possible at any time in BiSS or SSI protocol. However, for the transfer of angle data to the output register the incremental output is halted for one period of the clock signal at pin MA.

1. Max. Possible Converter Frequency Defined By The Maximum Input Frequency								
FCTR	Output Frequency fout @ fin_{max} **A, B**	Resolution Requirem. **bin**	**dec**	Maximum Input Frequency **fin_{max}**	Restrictions at high input frequency	Examples* fin_{max} [kHz] at resol. **8192**	**1024**	**200**
0x0004	325 kHz	X	X	fosc()min / 40 / Resolution	None	0.17	1.37	7.0
0x4102	542 kHz	X	X	fosc()min / 24 / Resolution	Relative angle error 2x increased	0.28	2.3	11.7
0x4202	1.08 MHz	X	X	2 x fosc()min / 24 / Res.	Relative angle error 4x increased	0.57	4.6	23.3
0x4302	2.17 MHz	X	X	4 x fosc()min / 24 / Res.	Relative angle error 8x increased	1.14	9.1	46.7
Notes	*) Calculated with fosc()min taken from Electrical Characteristics, item A02.							

Table 15: Maximum possible converter frequency for incremental A/B/Z output, defined by the maximum input frequency

2. Max. Possible Converter Frequency Defined By The Minimum Transition Distance						
FCTR	Output Frequency fout @ t_{MTD} **A, B**	Resolution Requirem. **bin**	**dec**	Minimum Transition Distance at A, B **t_{MTD}**	Restrictions at high input frequency	Example* t_{MTD} [µsec]
0x00FF	11 kHz	X	X	2048 / fosc()max	None	22.8
0x00FE	11.03 kHz	X	X	2040 / fosc()max	None	22.7
0x00FD	11.07 kHz	X	X	2032 / fosc()max	None	22.6
...	...	...	...	...	...	...
0x0006	402 kHz	X	X	56 / fosc()max	None	0.62
0x0005	536 kHz	X	X	48 / fosc()max	None	0.53
0x0004	562 kHz	X	X	40 / fosc()max	None	0.44
0x4102	938 kHz	X	X	24 / fosc()max	Relative angle error 2x increased	0.27
0x4202	1.87 MHz	X	X	12 / fosc()max	Relative angle error 4x increased	0.13
0x4302	3.75 MHz	X	X	6 / fosc()max	Relative angle error 8x increased	0.07
Notes	*) Calculated with fosc()max taken from El.Char., item A02; transition distance output A vs. output B with same direction of rotation.					

Table 16: Maximum possible converter frequency for incremental A/B/Z output, defined by the minimum transition distance

INCREMENTAL SIGNALS

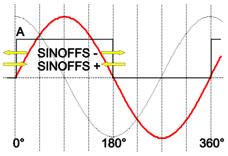
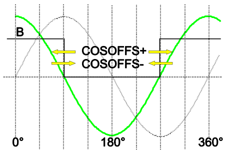
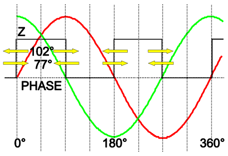
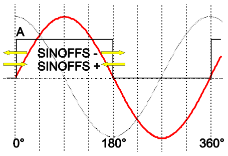
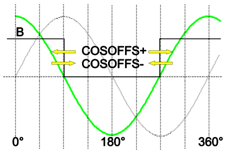
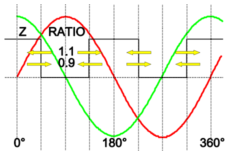
CFGABZ	Adr 0x02, Bit 3:2			
Code	Mode	Pin A	Pin B	Pin Z
0x00	Normal	A	B	Z
0x01	Control signals for external period counters	CA	CB	CZ
0x02	Calibration mode **Offset+Phase** The following settings are required additionally: SELRES = 0x0D ZPOS = 0x00 HYS = 0x07 ROT = 0x00 CFGAB = 0x00 AERR = 0x00	 Figure 5: Offset SIN*	 Figure 6: Offs. COS*	 Figure 7: Phase*
0x03	Calibration mode **Offset+Amplitude** The following settings are required additionally: SELRES = 0x0D ZPOS = 0x00 HYS = 0x07 ROT = 0x00 CFGAB = 0x00 AERR = 0x00	 Figure 8: Offset SIN*	 Figure 9: Offs. COS*	 Figure 10: Amplit.*
Notes	*) Trimmed accurately when duty cycle is 50 %; Recommended trimming order (after selecting GAIN): offset, phase, amplitude ratio, offset;			

Table 17: Outputs A, B, Z

ROT	Adr 0x02, Bit 5
Code	Code direction
0x00	Ascending order, B then A
0x01	Descending order, A then B

Table 18: Code direction

CBZ	Adr 0x02, Bit 4
Code	Reset via zero
0x00	Not activated
0x01	Activated

Table 19: Reset enable for period counter

ENRESDEL	Adr 0x02, Bit 7	
Code	Output*	Function
0x00	immediately	An external counter displays the absolute angle following power-on.
0x01	after 5 ms	An external counter only displays changes vs. the initial power-on (conditional on standby at power-on)
Notes	*) Output delay after device configuration and internal reset (A, B, Z remains on high).	

Table 20: Output delay A, B, Z

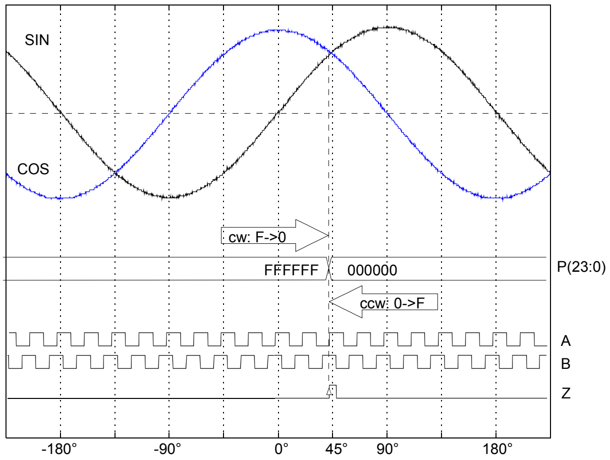


Figure 11: Period counter reset by zero signal (enabled by CBZ = 1).
Example gives a resolution of 64 (SELRES = 0x0A), a zero signal at 45° (ZPOS = 0x04, CFGAB = 0x00) and no inversion of the direction of rotation (ROT = 0x00, COS leads SIN).

ZPOS	Adr 0x01, Bit 4:0
Code	Position
0x00	0°
0x08	90°
0x10	180°
0x18	270°
0x01	11.25° (1 x 11.25°)
...	...
0x1F	348.75° (31 x 11.25°)
Notes	The zero signal is only output if released by the input pins (for instance with PZERO = 5 V, NZERO = VREF).

Table 21: Zero signal position

CFGZ	Adr 0x02, Bit 1:0
Code	Length
0x00	90°
0x01	180°
0x02.. 03	Synchronization

Table 22: Zero signal length

CFGAB	Adr 0x03, Bit 5:4
Code	Z = 1 for
0x00	B = 1, A = 1
0x01	B = 0, A = 1
0x02	B = 1, A = 0
0x03	B = 0, A = 0

Table 23: Zero signal logic

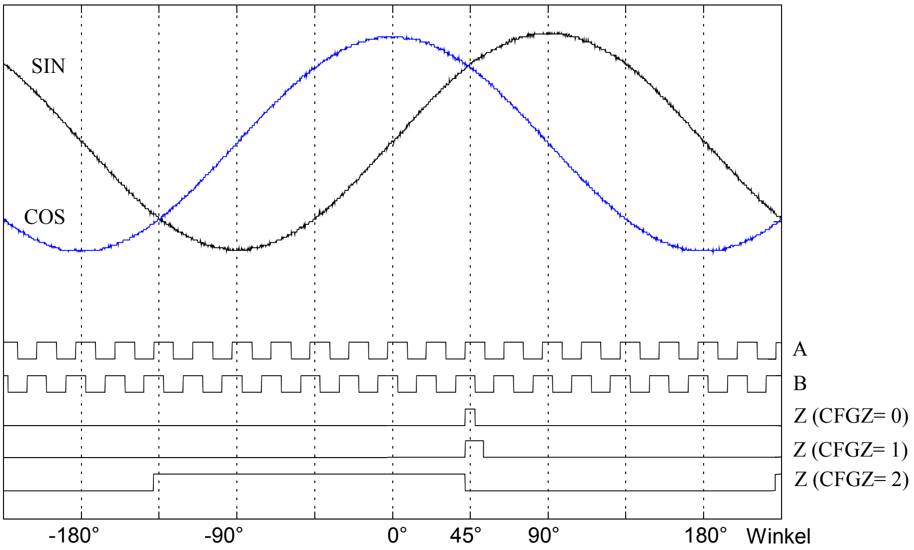


Figure 12: Incremental output signals for various zero signal lengths.
Example gives a resolution of 64 (SELRES = 0x0A), a zero signal position of 45° (ZPOS = 0x04, CFGAB = 0x00) and no inversion of the direction of rotation (ROT = 0x00, COS leads SIN).

SIGNAL MONITORING and ERROR MESSAGES

SELAMPL **AMPL**	Adr 0x0C, Bit 2 Adr 0x0C, Bit 1:0	
Max (|Sin| , |Cos|) for SELAMPL = 0		
Code	Voltage threshold V_{th}	Output amplitude*
0x00	0.60 x VDDA	1.4 V_{pp}
0x01	0.64 x VDDA	2.0 V_{pp}
0x02	0.68 x VDDA	2.6 V_{pp}
0x03	0.72 x VDDA	3.1 V_{pp}
$\mathbf{Sin^2 + Cos^2}$ for SELAMPL = 1		
Code	V_{thmin} ↔ V_{thmax}	Output amplitude*
0x04	(0.20 ↔ 0.9) x VDDA	1.0 V_{pp} ↔ 4.5 V_{pp}
0x05	(0.30 ↔ 0.9) x VDDA	1.5 V_{pp} ↔ 4.5 V_{pp}
0x06	(0.40 ↔ 0.9) x VDDA	2.0 V_{pp} ↔ 4.5 V_{pp}
0x07	(0.50 ↔ 0.9) x VDDA	2.5 V_{pp} ↔ 4.5 V_{pp}
Notes	V_{th}, V_{thmin}, V_{thmax} are typical values; refer to Elec. Char. No. H01 cf. for maximal values. *) Entries are calculated with VDDA = 5 V.	

Table 24: Signal amplitude monitoring

AERR	Adr 0x03, Bit 1
Code	Amplitude error message
0x00	disabled
0x01	enabled

Table 25: Amplitude error

FERR	Adr 0x03, Bit 0
Code	Excessive frequency error message
0x00	disabled
0x01	enabled
Notes	Input frequency monitoring is operational for resolutions $\geq$ 16

Table 26: Frequency error

Configuration error	
-	Always enabled

Table 27: Configuration error

Error Indication at NERR	
Failure Mode	Pin signal NERR
No error	HI
Amplitude error	LO/HI = 75 % (resp. HI for AERR = 0)
Frequency error	LO/HI = 50 % (resp. HI for FERR = 0)
Configuration	LO
Undervoltage	LO
System error	NERR = low caused by an external error signal

Table 28: Error indication at NERR

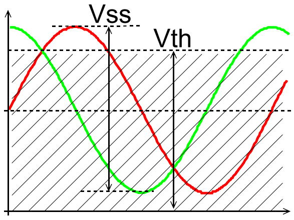


Figure 13: Signal monitoring of minimum amplitude.

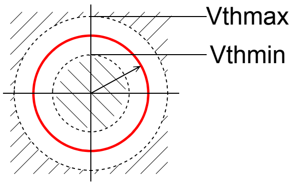


Figure 14: Sin^2 + Cos^2 signal monitoring.

Error Messages		
Failure Mode	Error bits E1, E0 for BiSS and SSI **CRC6 = 0**	Error bits nE, nW for BiSS and SSI **CRC6 = 1**
No error	1, 1	1, nW
Amplitude error	0, 1	0, nW
Frequency error	1, 0	0, nW
System error*	0, 0	0, nW
Warning**	—	nE, 0
Notes		
*System error	NERR pulled low by external signal	
**Warning	Automatic step-back of resolution	
Line Signal SLO	Data output is deactivated and SLO permanently high in case of: configuration phase, invalid configuration, undervoltage.	

Table 29: Error messages

To enable the diagnosis of faults, the various types of error are signaled at NERR using a PWM code as given in the key on the left.

Two error bits are provided to enable communication via the I/O interface; these bits can decode four different types of error. If NERR is held at low by an external source, such as an error message from the system, for example, this can also be verified via the I/O interface.

Error are stored until the sensor data is output via the I/O interface and then deleted. Errors at NERR are displayed for a minimum of ca. 10 ms unless they are deleted beforehand by a data output.

If an error in amplitude occurs, conversion is terminated and the incremental output signals halted. An error in amplitude rules out the possibility of an error in frequency.

TEST FUNCTIONS

TMODE	Adr 0x06, Bit 3:1	
Code	Signal at Z	Description
0x00	Z	no test mode
0x01	A xor B	Output A EXOR B
0x02	ENCLK	iC-Haus device test
0x03	NLOCK	iC-Haus device test
0x04	CLK	iC-Haus device test
0x05	DIVC	iC-Haus device test
0x06	PZERO - NZERO	iC-Haus device test
0x07	TP	iC-Haus device test
Condition	CFGABZ = 0x00	

Table 30: Test mode

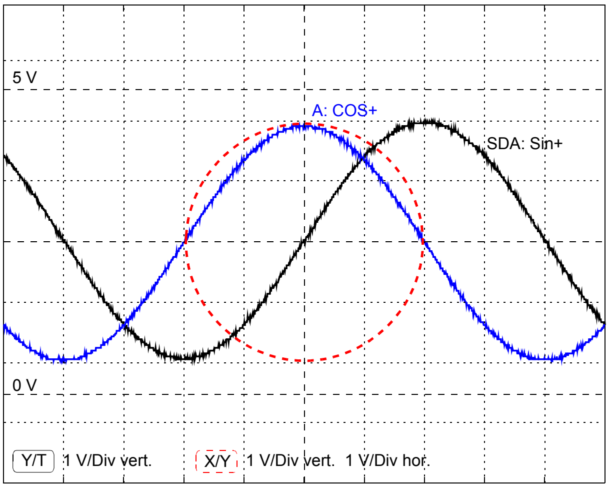


Figure 15: Calibrated signals in TMA mode.

TMA	Adr 0x06, Bit 0			
Code	**Pin A**	**Pin B**	**Pin SDA**	**Pin SCL**
0x00	A	B	SDA	SCL
0x01	COS+	COS-	SIN+	SIN-
Notes	To permit the verification of GAIN and OFFSET settings, signals are output after the input amplifier. A converter signal of 4 Vpp is the ideal here and should not be exceeded. Pin loads above 1 MΩ are adviceable for accurate measurements. EEPROM access is not possible during mode TMA.			

Table 31: Analog test mode

The signal is set to ca. 4 Vpp using GAIN and must not be altered after calibration. Both display modes are suitable for OFFS (positive values) and RATIO adjustments; X/Y mode is preferable for PHASE. Test signals COS- (pin B) and SIN- (pin SCL) must be selected to set negative values for OFFS.

I/O INTERFACE: BiSS C PROTOCOL

The serial I/O interface operates in BiSS C protocol mode and enables sensor data to be output in uninterruptible cycles (data channel SCD). At the same time parameters can be exchanged via bidirectional register communication (data channel CD).

The sensor data produced by iC-NQC contains the angle value (S) with 3 to 13 bits, the period count (P) with 0, 8, 12 or 24 bits, two error bits (E1 and E0) and 5 or 6 CRC bits (CRC).

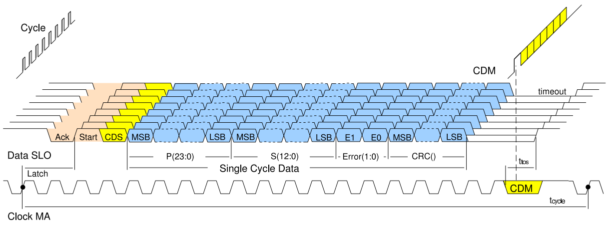


Figure 16: Example line signals (BiSS C)

Single Cycle Data Channel: SCD		
Bits	Typ	Label
0...24	DATA	Period counter P(23:0): 0, 8, 12, 24 bit (multiturn position)
3...13	DATA	Angle data S(12:0): 3 bis 13 bit (singleturn position)
1	ERROR	Error bit E1 (amplitude error)
1	ERROR	Error bit E0 (frequency error)
5...6	CRC	Polynomial 0x25 $x^5 + x^2 + x^0$ (inverted bit output) - oder - Polynomial 0x43 $x^6 + x^1 + x^0$ (inverted bit output)

Table 32: BiSS data channels

Interface Parameters With BiSS C Protocol

SELSSI	Adr 0x02, Bit 6	
Code	Protocol	Information
0 1	BiSS C SSI	BiSS INTERFACE *www.biss-interface.com*

Table 33: Protocol version

TIMO	Adr 0x06, Bit 5		
Code	Clock	Timeout t_{tos}	fclk(MA) min*
0	46-47	ca. 20 µs	50 kHz
1	3-4	ca. 1.5 µs	660 kHz
TOA	Addr 0x07, Bit 3		
0	see TIMO		
1	adaptive with T_{CLK} = 42/fosc	see BiSS specification	50 kHz
Notes	A ref. clock count is equal to $\frac{32}{fosc}$ (see El. Char., A02). The permissible max. clock frequency is specified by E06. *) A low clock frequency can reduce the permissible maximum input frequency since conversion is paused for one MA cycle from *Latch* onwards.		

Table 34: Timeout configuration (protectable)

M2S	Adr 0x00, Bit 6:5	
Code	Data Length	CRC Polynomial
0x00	-	0x25 (with CRC6 = 0)
0x01	P(7:0)	0x25 (with CRC6 = 0)
0x02	P(11:0)	0x43
0x03	P(23:0)	0x43

Table 35: Period counter output

CRC6	Adr 0x03, Bit 7	
Code	CRC Polynomial	Status Messages
0	determined by M2S	E1, E0
1	0x43	nE, nW

Table 36: CRC polynomial

NZB	Adr 0x03, Bit 6
Code	Function
0	Zero bit
1	No zero bit
Notes	The optional zero bit is output as the final bit after the CRC.

Table 37: Zero bit

ENCDS	Adr 0x00, Bit 7
Code	Description
0x00	Data output BiSS B or SSI
0x01	Data output BiSS C

Table 38: Protocol options

M2S can be used to set the number of period counter bits sent as sensor data. The counter bits are transmitted before the angle value, with the MSB leading.

The 5-bit CRC output is based on polynomial 0x25 (100101b), with the 6-bit CRC output based on polynomial 0x43 (1000011b) automatically coming active with longer SCD data, or when preselected by CRC6. As a rule, CRC bits are sent inverted.

An additional zero bit can be output following the CRC bits. However, disabling the zero bit by NZB = 1 is recommended when the output data length does not need to comply with existing applications.

To obtain a position data output being compatible to the BiSS B protocol parameter ENCDS = 0 does switch off the CDS bit, without a replacement by a zero bit. Thus, the output data length is shorten by one bit and register communication is limited to the direction of the master to the slave. The bidirectional BiSS C register communication must be enabled by setting ENCDS = 1.

Example Of BiSS Data Output

SCD: Angle data		
Bits	Typ	Label
12	DATA	Angle data S(11:0)
2	ERROR	Error nE and warning nW
6	CRC	Polynomial 0x43
Config.	SELRES = 0x04, M2S = 0x00, CRC6 = 1, NZB = 1	

Table 39: Example format 1 for BiSS profile BP1

SCD: Angle data with 8-bit period count		
Bits	Type	Label
8	DATA	Period counter P(7:0)
13	DATA	Angle data S(12:0)
2	ERROR	Error bits E1, E0
5	CRC	Polynomial 0x25
1	Zero	Zero bit
Config.	SELRES = 0x03, M2S = 0x01, CRC6 = 0, NZB = 0	

Table 40: Example format 2

SCD: Angle data with 24-bit period count		
Bits	Type	Label
24	DATA	Period counter P(23:0)
13	DATA	Angle data S(12:0)
2	ERROR	Error bits E1, E0
6	CRC	Polynomial 0x43 (no zero bit)
Config.	SELRES = 0x03, M2S = 0x03, CRC6 = 0, NZB = 1	

Table 41: Example format 3

Register Communication

After the BiSS C protocol slave registers are directly addressed in a reserved address area (0x40 to 0x7F). Other storage areas are addressed dynamically and in blocks. BiSS addresses 0x00 to 0x3F aim for a register bank consisting of 64 bytes, the physical storage address of which is determined by Bank Select n.

iC-NQC supports up to 16 storage banks, making it possible to use an 8-bit EEPROM to its full capacity. There is therefore also enough storage space for an ID plate (EDS) and OEM data.

Information regarding memory map and addressing via BiSS is given on page 25).

Internal Reset Function

A write access at RAM address 0x00 (BiSS address 0x00 with Bank Select n = 0) triggers an internal reset.

Based on the current configuration in the RAM, iC-NQC restarts without reading the EEPROM. The configured interface timeout and write protect settings become active, the period counter is set to zero and any stored configuration errors are deleted. The data output via SLO and the incremental signals at A, B and Z are released. Providing no amplitude error is present, the converter again counts up from an angle value of zero to the current angle position.

Short BiSS Timeout

For programming via the I/O interface iC-NQC has a short BiSS timeout function according to the description of the BiSS C protocol (see page 19, Table 2, El. Char. no. 6).

Regardless of register protection settings a short timeout of typically 1.8 µs can be temporarily activated by writing value 0x07 to address 0x7C (address 124d). A controller can then transmit the device configuration over a shorter period.

TOS	Adr 0x7C, Bit 2:0
Code	Function
000	Regular timeout (configured by TIMO)
001...111	Short timeout (equal to TIMO = 1)

Table 42: Short timeout (via BiSS device ID)

The value written to address 0x7C is also transferred to the EEPROM, provided an EEPROM has been connected up and is available.

On reading address 0x7C the byte stored in the EEPROM is output as part of the BiSS device ID. Here, high-order bits 7:3 are part of the manufacturer's ID; low-order bits 2:0 act as an indicator of the timeout options (regular or short timeout, see Table 42).

I/O INTERFACE: SSI Protocol

iC-NQC can transmit position data in SSI protocol mode; the parameters described in the following give the necessary settings and options.

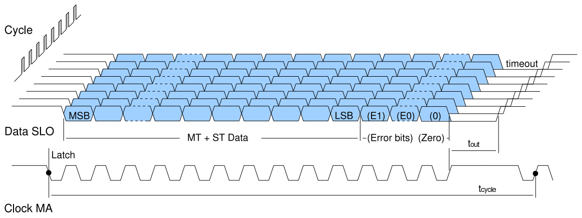


Figure 17: Example line signal (SSI)

SELSSI	Adr 0x02, Bit 6
Code	Protocol
0	BiSS C
1	SSI

Table 43: Protocol version

TIMO	Adr 0x06, Bit 5	
Code	Timeout t_{tos}	fclk(MA)min*
0	Long: ca. 20 µs	50 kHz
1	not permitted	
TOA	Adr 0x07, Bit 3	
0	see TOS	
1	not permitted	
Notes	A ref. clock count is equal to $\frac{32}{fosc}$ (see El. Char. A02). The permissible max. clock frequency is specified by item E06. *) A low clock frequency can reduce the permissible maximum input frequency since conversion is paused for one MA cycle from *Latch* onwards.	

Table 44: Timeout configuration for SSI

M2S	Adr 0x00, Bit 6:5
Code	Period counter output length
0x00	-
0x01	P(7:0)
0x02	P(11:0)
0x03	P(23:0)

Table 45: Period counter for SSI data output

CRC6 **NZB**	Adr 0x03, Bit 7 Adr 0x03, Bit 6	
Code	Additional bits	Ring operation
0 0	E1, E0	no
0 1	none	no
1 0	nE, nW, zero bit	yes
1 1	none	yes

Table 46: Options for SSI data output

GRAY	Adr 0x05, Bit 7
Code	SSI data format
0	binary coded
1	gray coded
Notes	Data output starts with MSB for binary or Gray coded data.

Table 47: SSI data format

Examples Of SSI Data Output

SSI Output Formats																						
13-bit SSI																						
Res	**Mode**	**Error**	**CRC**	**T1**	**T2**	**T3**	**T4... T10**	**T11**	**T12**	**T13**	**T14**	**T15**	**T16**	**T17**	**T18**	**T19**	**T20**	**T21**	**T22**	**T23**	**T24**	**T25**
10 bit	SSI	X	-	S9	S8	S7	S6 ... S0	E1	E0	0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
			Example							0	0	0	0	0	0	0	0	0	0	0	0	0
13 bit	SSI *1	-	-	S12	S11	S10	S9 ... S3	S2	S1	S0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
			Example								0	0	0	0	0	0	0	0	0	0	0	0
	SSI-R *2	-	-	S12	S11	S10	S9 ... S3	S2	S1	S0	Stop	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2
			Example								0											
25-bit SSI																						
13 bit	SSI	X	-	S12	S11	S10	S9 ... S3	S2	S1	S0	E1	E0	0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
			Example										0	0	0	0	0	0	0	0	0	0
8 + 13 bit^{*3}	SSI	X	-	P7	P6	P5	P4 ... P0, S12, S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	E1	E0	0	Stop
			Example																		0	0
			Configuration	Input SLI = 0, SELSSI = 1, M2S = 0x00, CRC6 = 0, NZB = 0, unless otherwise noted. *1) CRC6 = 0, NZB = 1; *2) CRC6 = 1, NZB = 1; *3) M2S = 0x01																		
			Caption	SSI = SSI protocol SSI-R = SSI ring operation																		

Table 48: SSI transmission formats

EEPROM INTERFACE

The serial EEPROM interface consists of the two pins SCL and SDA and enables read and write access to a serial EEPROM with I^{2}C interface (with at least 128 bytes, 5 V type with a 3.3 V function; e.g. 24C01, 24C02, 24C08 and maximal 24C16).

The configuration data in the EEPROM, of addresses 0x00 to 0x0F, is secured by a CRC check value to address 0x0F. When the device is powered up, the address range from 0x00 to 0x0F is mapped onto iC-NQC's configuration RAM. The higher memory area contains BiSS C slave registers and optional memory banks available to the sensor system.

The register access to the configuration data and the memory banks 1 to 7 (intended for EDS) can be restricted by parameter RPL.

N.B. When writing configuration data to the EEPROM (BiSS addresses 0x10 to 0x1F) a wait time of at least 4 ms must be allowed after each register.

Example of CRC Calculation Routine

```
unsigned char ucDataStream = 0;
int iCRCPoly = 0x127;
unsigned char ucCRC=0;
int i = 0;

ucCRC = 0; // start value !!!
for (iReg = 0; iReg<15; iReg ++)
{
  ucDataStream = ucGetValue(iReg);
  for (i=0; i<=7; i++) {
    if ((ucCRC & 0x80) != (ucDataStream & 0x80))
      ucCRC = (ucCRC << 1) ^ iCRCPoly;
    else
      ucCRC = (ucCRC << 1);
    ucDataStream = ucDataStream << 1;
  }
}
```

CRC_E2P	Adr 0x0F, Bit 7:0
Code	Description
0x00 ... 0xFF	Check value formed by CRC polynomial 0x127

Table 49: Check value for EEPROM data

Register Configuration		
BiSS Adr hex	BiSS Adr decimal	Contents
0x00...0F	0...15	Config. Data RAM (16 bytes)
0x10...1F	16...31	Config. Data EEPROM (16 bytes)
0x20...3F	32...63	Unused memory area (32 bytes)
BiSS C Slave-Registers (direct addresses):		
0x40	64	Bank Select (1 byte)
0x41	65	EDS Bank (1 byte)
0x42...43	66...67	Profile ID (2 bytes)
0x44...47	68...71	Serial No. (4 bytes)
0x48...77	72...119	Slave Registers (48 bytes)
		Device ID (6 bytes):
0x78	120	4E (default)
0x79	121	51 (default)
0x7A	122	43 (default)
0x7B	123	31 (default)
0x7C	124	Bit 7:3: Adr 0x00, Bit 2:0: TOS
0x7D	125	00 (default)
		Manufacturer's ID (2 bytes):
0x7E	126	69 (default)
0x7F	127	43 (default)

Table 50: Register overview

RPL	Adr 0x03, Bit 3			
Code	Bank 0 Config. Dat.	0x40..7F BiSS ID	Bank 1..7 EDS	Bank 8..15 User Data
0x0	read / write	read / write	read / write	read / write
0x1	-	read*	read	read / write
Notes	*) Exception: write to 0x40 and 0x7C is always possible.			

Table 51: Register protection settings

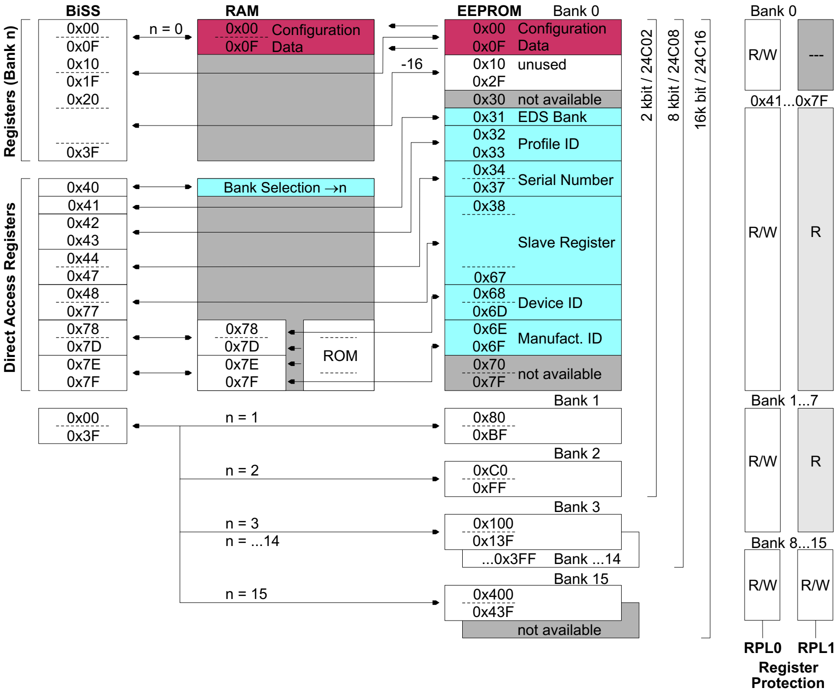


Figure 18: Registers and addressing

STARTUP BEHAVIOR

Startup with a configured EEPROM
After the supply has been turned on (power-on reset), iC-NQC reads the configuration data from the EEPROM. During this phase it actively keeps error pin NERR at a low signal (open drain output), and data output SLO and the incremental signals at A, B and Z at a high signal.

After a successful CRC the data output to SLO and to the incremental A, B, and Z outputs is released and the error indication at pin NERR reset; an external pull-up resistor at pin NERR can supply a high signal. iC-NQC then switches to normal operation and determines the current angle position, providing that a sensor is connected up to it and there is no amplitude error (or this is deactivated).

Should the CRC prove unsuccessful due to a data error (disrupted transmission, no EEPROM or the EEPROM is not programmed), the configuration phase is automatically repeated. After a third failed attempt, the procedure is aborted and error pin NERR displays a permanent low; data output SLO and the incremental signals at A, B and Z remain at a high signal.

Startup without an EEPROM
The configuration RAM contains random values after startup; iC-NQC does not have a default configuration. Error pin NERR shows a low signal (open drain output); data output SLO and the incremental signals at A, B and Z indicate a high signal.

To reduce the device configuration time, a short timeout of 3 µs maximum (cf. TIMO = 1 and TOA = 0) can be temporarily activated by writing value 0x07 to address 0x7C (address 124d).

When operated without an EEPROM, iC-NQC does not respond to higher addresses - with the exception of the BiSS addresses reserved for manufacturer and device IDs (0x78 to 0x7F). This address area supplies the chip version from the ROM.

Initialization after configuration failure
So that it is always possible to talk to iC-NQC via the I/O interface, iC-NQC first ignores the register values of TIMO, TOA, RPL and TMA. Instead, iC-NQC applies the longest timeout (cf. TIMO = 0 and TOA = 0), ignores safety settings (cf. RPL = 0x0) and evaluates the BiSS register communication (CDM bit from the CD data channel).

During this phase regular bidirectional BiSS register communication is not yet possible, as data output SLO is permanently kept at high. Writing the configuration to RAM addresses 0x01 to 0x0C and to address 0x00 must be executed without evaluating a reply. Data input SLI is ignored; iC-NQC always uses slave ID 0.

Each cycle transmits a single bit only and can be reduced to four clocks plus the timeout (CDM). The following figures each show a single cycle with CDM = 0 and CDM = 1. A wide range of 100 ns to 12.5 µs is permissible for clock period T(MA); the timeout must last at least 30 µs.

A complete write cycle requires 14 cycles at CDM = 0 and a sequence of 32 cycles calculated according to BiSS-C register communication.

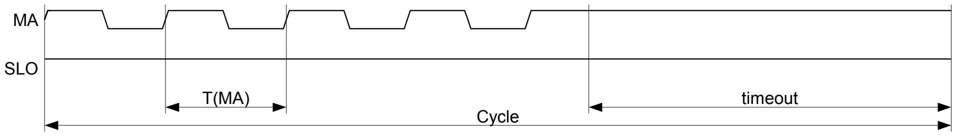


Figure 19: BiSS cycle at CDM = 0

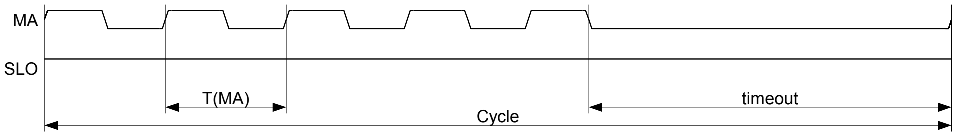


Figure 20: BiSS cycle at CDM = 1

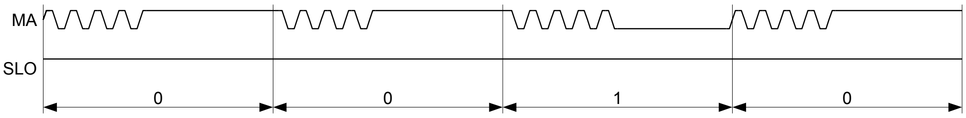


Figure 21: BiSS cycle extract for a CDM sequence of ’0010’.

Ahead of a write access to address zero finishing the initialization phase and setting the BiSS interface to normal operation, at least the following register bits need to be reset: SELSSI at address 0x02, RPL at address 0x03, and TMA and TIMO at address 0x06.
The following sequence gives an example of programming addresses 0x02, 0x03 and 0x06 to zero and subsequently executing a reset by programming address 0x00 with a value of 0x8D (141d).

"00000000000000"
"11000000001000000110000000011110"
"00000000000000"
"11000000001100110110000000011110"
"00000000000000"
"11000000011011000110000000011110"
"00000000000000"
"11000000000001100111000110101010"

Notes: Data output SLO is only operational following initialization. The controller needs to execute the described initialization without any feedback (sending CDM bits without evaluating CDS bits).

N.B.: CDM bits are inverted on the line; when CDM = 1 the timeout is at low.

Programming tip: After writing a byte to the EEPROM the same byte should be read back. When doing so, iC-NQC does not output the start bit if the EEPROM is busy with its internal write procedure and so denies I2C access. Several read attempts may be required if the I2C interface is still blocked causing iC-NQC to refuse the read access.
When writing to the EEPROM without reading the byte back, a wait time of at least 4 ms must be allowed after each register.

APPLICATION NOTES

Principle input circuits

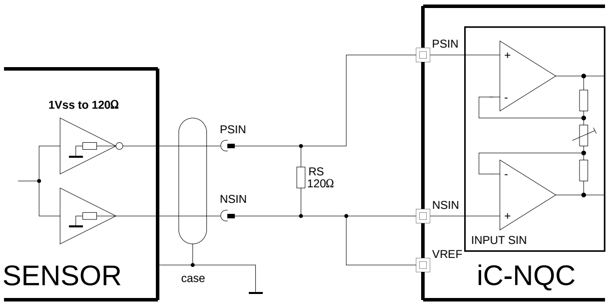


Figure 22: Input circuit for voltage signals of 1 Vpp with no ground reference. When ground is not separated the connection NSIN to VREF must be omitted.

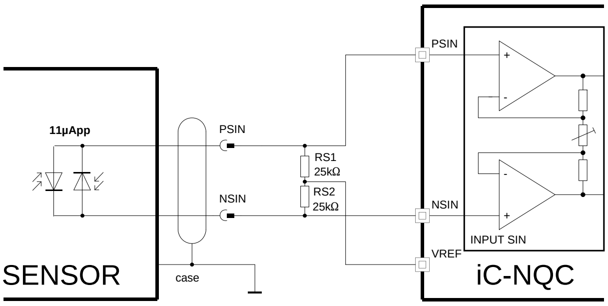


Figure 23: Input circuit for current signals of 11 µA with no ground reference. Offset calibration is not possible with this circuit.

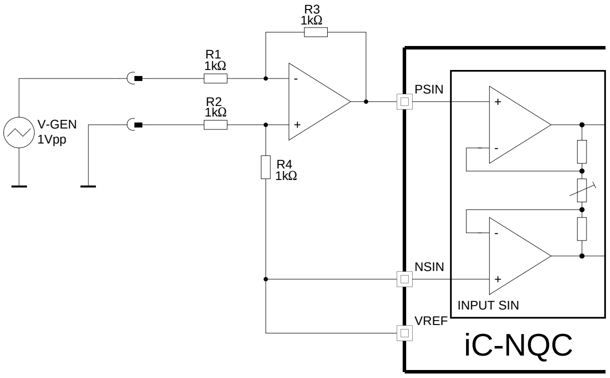


Figure 24: Input circuit for non-symmetrical voltage or current source signals with ground reference (adaptation via resistors R3, R4).

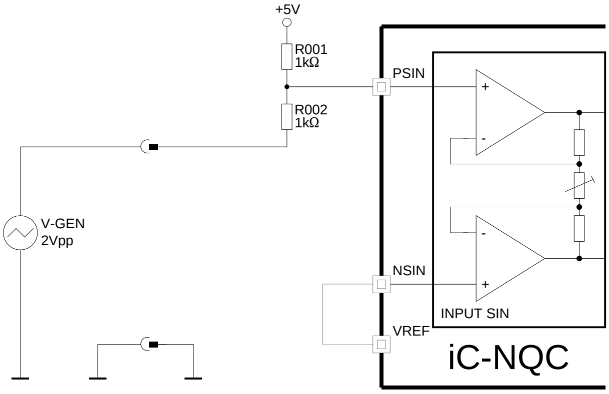


Figure 25: Simplified input wiring for non-symmetrical voltage signals with ground reference.

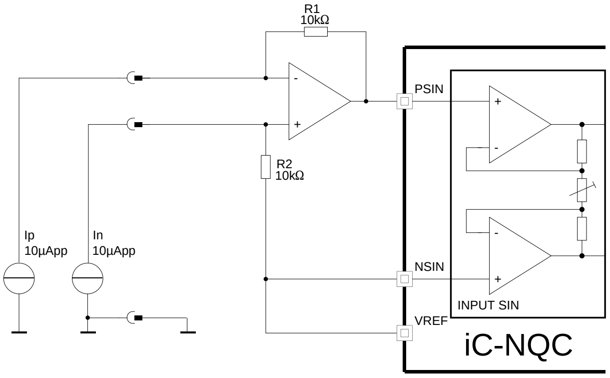


Figure 26: Input circuit for complementary low-side current source outputs, such as for optoencoder iC-WG.

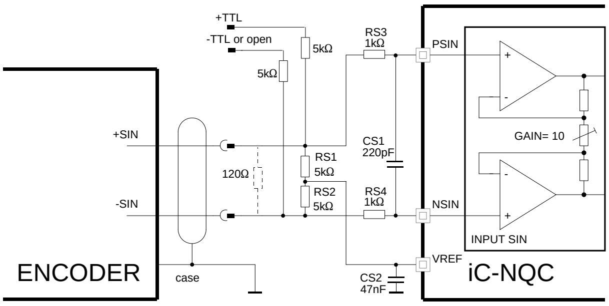


Figure 27: Combined input circuit for 11 µA, 1 Vpp (with 120 Ω termination) or TTL encoder signals. RS3/4 and CS1 serve as protection against ESD and transients.

Basic circuit

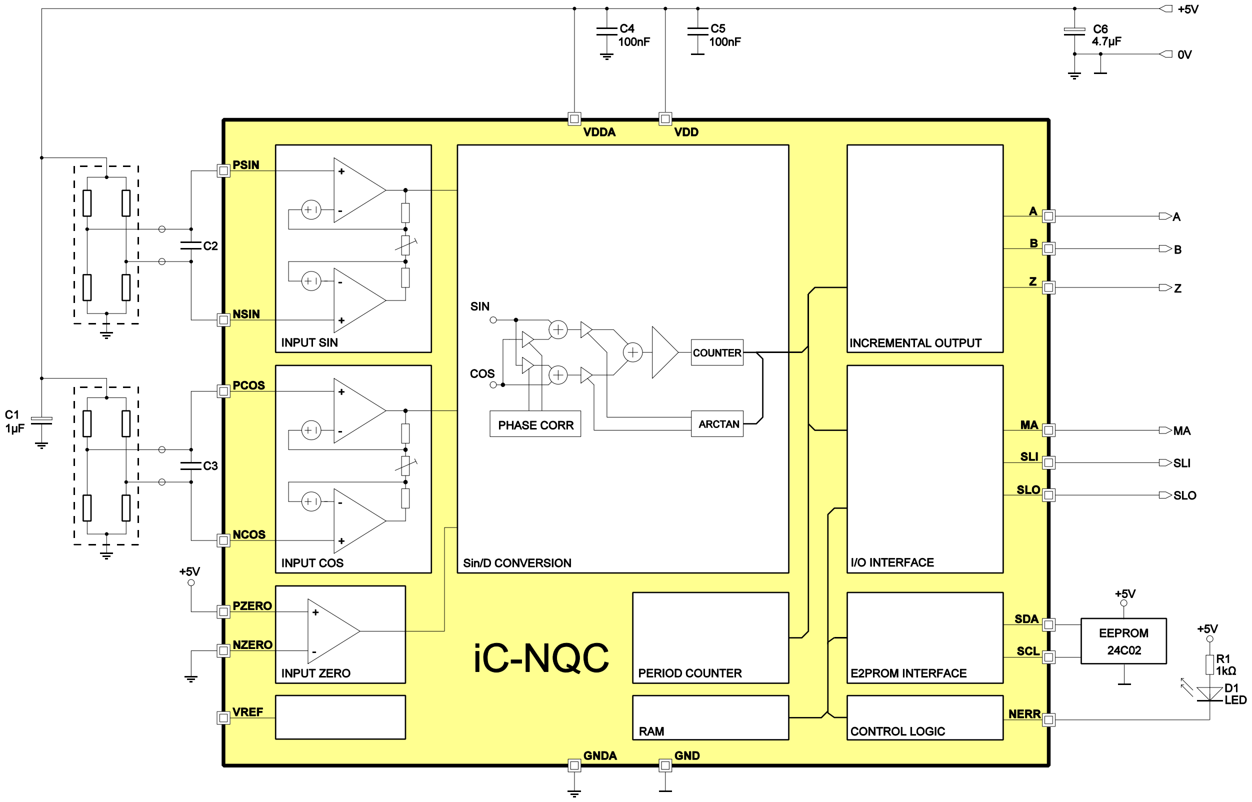


Figure 28: Basic circuit for the evaluation of MR bridge sensors.

EVALUATION BOARD

iC-NQC comes with a demo board for test purposes.
Instructions are available separately.

DESIGN REVIEW: Function Notes

iC-NQC 2		
No.	Function, Parameter/Code	Description and Application Notes
		Please refer to datasheet release B1.

Table 52: Notes on chip functions regarding iC-NQC chip release 2.

iC-NQC 3		
No.	Function, Parameter/Code	Description and Application Notes
1	**GRAY**	For Gray-coded data output clock cycles must be fully completed. An earlier termination results in invalid data for the following read out cycle.
2	**Startup**	An invalid CRC keeps only SLO permanently on high, the incremental output to A, B and Z is not blocked.

Table 53: Notes on chip functions regarding iC-NQC chip release 3.

iC-NQC 5		
No.	Function, Parameter/Code	Description and Application Notes
1	**GRAY**	Gray-coded data output can be terminated at any time.
2	**Startup**	An invalid CRC keeps SLO and A, B and Z permanently on high (until an internal reset).
3	**Period counting**	Following power-on and after an internal reset the period counter is initialized with a value of zero (as all former chip releases). If an input angle of exactly 0° is applied and a movement towards 270° is following, the period counter counts to the value -1 (former chip releases maintain the value of zero).

Table 54: Notes on chip functions regarding iC-NQC chip release 5.

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We understand suitable application of our published designs to be state-of-the-art technology which can no longer be classed as inventive under the stipulations of patent law. Our explicit application notes are to be treated only as mere examples of the many possible and extremely advantageous uses our products can be put to.

ORDERING INFORMATION

Type	Package	Order Designation
iC-NQC	TSSOP20 4.4 mm	iC-NQC TSSOP20
Evaluation Board		iC-NQC EVAL NQ6D

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