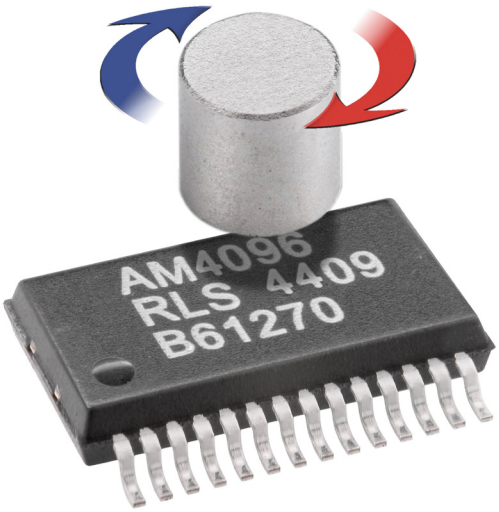
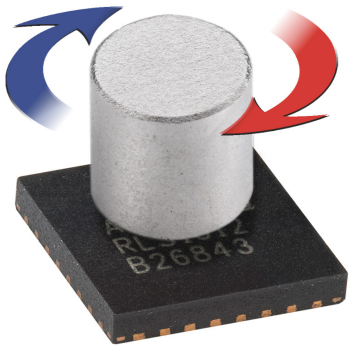
Data sheet
AM4096D02_09
Issue 9, 30th November 2021

AM4096 – 12 bit angular magnetic encoder IC



AM4096
(SMD package SSOP28)



AM4096Q
(SMD package QFN32)

The AM4096 uses Hall sensor technology for sensing the magnetic field.

A circular array of sensors detects the perpendicular component of the magnetic field. The signals are summed then amplified. Sine and cosine signals are generated when the magnet rotates. The sine and cosine signals are factory calibrated for optimum performance.

From the sine and cosine values the angular position is calculated with a fast 12 bit interpolator. The calculated position is then output in various digital and analogue formats.

An inbuilt voltage regulator ensures stable conditions for the core of the chip and a more flexible power supply voltage. All inputs and outputs are related to the external supply voltage.

The AM4096 has many different setting options which are defined by the contents of internal registers. The zero position can be also set with an external pin. The settings of the chip are stored in an integrated EEPROM. The registers and the EEPROM can be accessed through a serial two wire interface TWI.

With its compact size the AM4096 is especially suitable for different applications, including motor motion control and commutation, robotics, camera positioning, various encoder applications, battery powered devices and other demanding high resolution applications.

Output options:
- Incremental
- Serial SSI
- Serial two wire interface (TWI)
- UVW commutation output
- Linear voltage
- Tacho
- Analogue sinusoidal

- **Contactless angular position encoding over 360°**
- **12 bit absolute encoder**
- **Presetable zero position**
- **High speed operation to 60,000 rpm**
- **Power save mode for low current consumption**
- **5 V or 3 V power supply**
- **Integrated EEPROM**

Block diagram

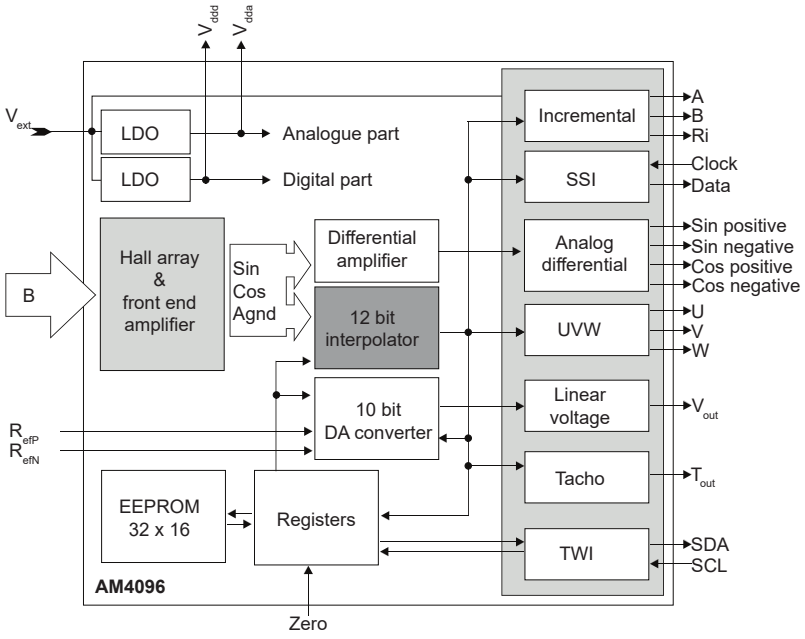


Fig. 1: AM4096 block diagram

Pinout for AM4096 (SSOP28)

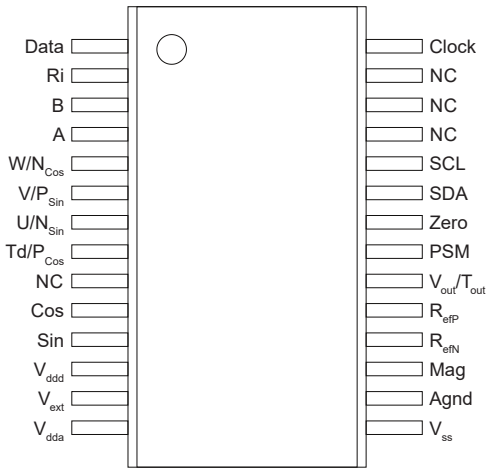


Fig. 2: Pin description for AM4096

Pinout for AM4096Q (QFN32)

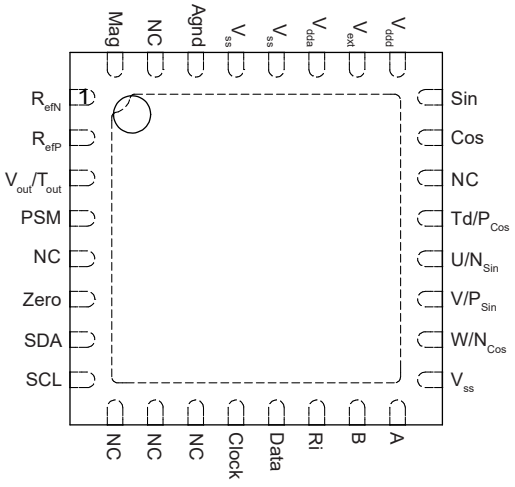


Fig. 3: Pin description for AM4096Q

Pinout for AM4096 (SSOP28)

continued

Pin	Name	Pin description
1	Data	SSI data output
2	Ri	Incremental output Ri
3	B	Incremental output B
4	A	Incremental output A
5	W/N_{Cos}	Commutation output W/Cosine negative output
6	V/P_{Sin}	Commutation output V/Sine positive output
7	U/N_{Sin}	Commutation output U/Sine negative output
8	Td/P_{Cos}	Tacho direction output/Cosine positive output
9	NC	Factory test
10	Cos	Cosine analogue output for filtering
11	Sin	Sine analogue output for filtering
12	V_{ddd}	Digital power supply 3.0 / 3.3 V
13	V_{ext}	Power supply input 5 V
14	V_{dda}	Analogue power supply 3.0 / 3.3 V
15	V_{ss}	Power supply 0 V
16	Agnd	Analogue reference voltage
17	Mag	Output, that indicates magnet presence
18	R_{efN}	Lower reference input for voltage output
19	R_{efP}	Upper reference input for voltage output
20	V_{out}/T_{out}	Linear voltage output/Tacho output
21	PSM	Power save mode input
22	Zero	Zeroing input
23	SDA	TWI serial interface data line
24	SCL	TWI serial interface clock line
25	NC	Factory test
26	NC	Factory test
27	NC	Factory test
28	Clock	SSI clock input

Pinout for AM4096Q (QFN32)

continued

Pin	Name	Pin description
1	R_{efN}	Lower reference input for voltage output
2	R_{efP}	Upper reference input for voltage output
3	V_{out}/T_{out}	Linear voltage output/Tacho output
4	PSM	Power save mode input
5	NC	Factory test
6	Zero	Zeroing input
7	SDA	TWI serial interface data line
8	SCL	TWI serial interface clock line
9	NC	Factory test
10	NC	Factory test
11	NC	Factory test
12	Clock	SSI clock input
13	Data	SSI data output
14	Ri	Incremental output Ri
15	B	Incremental output B
16	A	Incremental output A
17	V_{ss}	Power supply 0 V
18	W/N_{Cos}	Commutation output W/Cosine negative output
19	V/P_{Sin}	Commutation output V/Sine positive output
20	U/N_{Sin}	Commutation output U/Sine negative output
21	Td/P_{Cos}	Tacho direction output/Cosine positive output
22	NC	Factory test
23	Cos	Cosine analogue output for filtering
24	Sin	Sine analogue output for filtering
25	V_{ddd}	Digital power supply 3.0/3.3 V
26	V_{ext}	Power supply input 5 V
27	V_{dda}	Analogue power supply 3.0/3.3 V
28	V_{ss}	Power supply 0 V
29	V_{ss}	Power supply 0 V
30	Agnd	Analogue reference voltage
31	NC	Factory test
32	Mag	Output, that indicates magnet presence

Pin description

Some pins have more than one function. The function of those pins can be selected over two wire serial interface and stored in the chip. All digital pins have a pull-down resistor except PSM pin.

Name	Pin description
Data	a digital output for serial SSI communication
Ri	the quadrature incremental reference mark output
B	the quadrature incremental output B
A	is the quadrature incremental output A
W/N_{Cos}	the commutation digital output W or analogue differential buffered Cosine negative output
V/P_{Sin}	the commutation digital output V or analogue differential buffered Sine positive output
U/N_{Sin}	the commutation digital output U or analogue differential buffered Sine negative output
Td/P_{Cos}	the tacho direction digital output or analogue differential buffered Cosine positive output
Cos	the single-ended cosine analogue output for filtering
Sin	the single-ended sine analogue output for filtering
V_{ddd}	the pin for filtering the power supply of the digital part of the chip. The power supply voltage is selectable between 3 V and 3.3 V
V_{ext}	the external power supply pin (3 V to 5.5 V)
V_{dda}	the pin for filtering the power supply of the analogue part of the chip. The power supply voltage is selectable between 3 V and 3.3 V
V_{ss}	the power supply pin 0 V
Agnd	the pin for filtering analogue reference voltage (1.55 V)
Mag	the digital output for monitoring the magnet presence. If the output is high than the magnet distance is OK. If the distance is too small or too large, then the output voltage is low
R_{efN}	the reference voltage input for defining the minimum output value of the linear voltage output
R_{efP}	the reference voltage input for defining the maximum output value of the linear voltage output
V_{out}/T_{out}	the linear voltage output or tacho output
PSM	the digital input pin for power save mode operation. The input is floating and it must have defined input. When the input is low, the power save mode is inactive
Zero	the digital input for zeroing the output position with internal 10k pull-down resistor. The zeroing is done at transition from low to high
SDA	the data line for the two wire serial interface (TWI)
SCL	the clock line for the two wire serial interface (TWI)
NC	Test pins and must be left unconnected
Clock	the digital clock input for SSI communication with internal 10k pull-down resistor

Technical specifications

Absolute maximum ratings

T_A = 22 °C unless otherwise noted.

Parameter	Symbol	Min.	Max.	Unit	Note
Supply voltage	V_{ext}	–0.3	5.5	V	
Input pin voltage	V_{in}	–0.3	5.5	V	
Input current (latch-up immunity)	I_{scr}	–100	100	mA	
Electrostatic discharge	ESD		2	kV	*
Operating junction temperature	T_j	–40	140	°C	
Storage temperature range	T_{st}	–40	150	°C	
Moisture sensitivity level			3		

* Human Body Model

Operating range conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
General						
Temperature range	T_O	–40	125		°C	
Temperature range for EEPROM write	T_{OE}	–40	115		°C	
Supply voltage	V_{ext}	3	5	5.5	V	
Supply current	I_{dd}	*	26	30	mA	*
Power-up time	t_p		1.5	2	ms	
Interpolator delay	t_{di}		0.7		µs	
Sensors delay	t_{ds}		10		µs	
Filtering delay	t_{df}		20		µs	**
Oscillator						
Oscillator frequency	f_{osc}	8	10	12	MHz	
Oscillator frequency temperature drift	TC_{osc}		–0.006		% / K	
f_{osc} power supply dependence	VC_{osc}		3		% / V	***
Digital outputs						
Saturation voltage hi (V_{ext} – V_{out})	V_{shi}	137		490	mV	I_{load} = 2mA
Saturation voltage lo	V_{slo}	124		339	mV	I_{loa} = 2mA
Rise time	t_r	4		12	ns	C_{load} = 15+3pF
Fall time	t_f	3		9	ns	C_{load} = 15+3pF
Digital inputs						
Threshold voltage hi	Vt_{hi}	0.39	0.5	0.59	V_{ext}	
Threshold voltage lo	Vt_{lo}	0.30	0.38	0.45	V_{ext}	
Hysteresis	Vt_{hys}	0.08	0.12	0.15	V_{ext}	

* When in power-save mode the average supply current is significantly reduced.
** Typical time delay is calculated for filter capacitors 10 nF.
*** Due to internal supply regulator only 3 V or 3.3 V is possible.

AM4096 programming

The AM4096 can be programmed over the two-wire serial interface (TWI) which is compatible with I²C protocol with a 400 kbps bit rate speed.

The TWI protocol allows the to interconnect up to 128 individually addressable devices using only two bi-directional bus lines, one for clock (SCL) and one for data (SDA). The only external hardware needed to implement the bus is a single pull-up resistor for each of the TWI bus lines. All devices connected to the bus have individual addresses, and mechanisms for resolving bus contention are inherent in the TWI protocol.

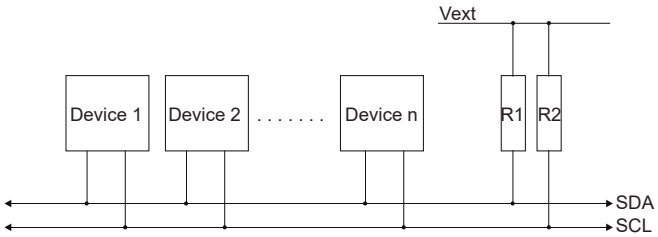


Fig. 4: TWI bus interconne

The TWI bus is a multi-master bus where one or more devices, capable of taking control of the bus, can be connected. Only Master devices can drive both the SCL and SDA lines while a Slave device is only allowed to issue data on the SDA line. Data transfer is always initiated by a Bus Master device. A high to low transition on the SDA line while SCL is high is defined to be a START condition (or a repeated start condition).

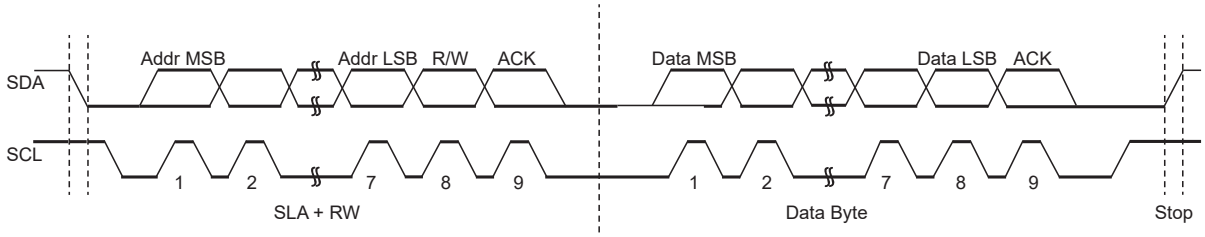


Fig. 5: TWI Address and Data Packet Format

A START condition is always followed by the (unique) 7 bit slave addresses and then by a Data Direction bit. The Slave device addressed now acknowledges to the Master by holding SDA low for one clock cycle. If the Master does not receive any acknowledge the transfer is terminated. Depending of the Data Direction bit, the Master or Slave now transmits 8 bit of data on the SDA line. The receiving device then acknowledges the data. Multiple bytes can be transferred in one direction before a repeated START or a STOP condition is issued by the Master. The transfer is terminated when the Master issues a STOP condition. A STOP condition is defined by a low to high transition on the SDA line while the SCL is high. If a Slave device cannot handle incoming data until it has performed some other function, it can hold SCL low to force the Master into a wait-state. All data packets transmitted on the TWI bus are 9 bits long, consisting of one data byte and an acknowledge bit. During a data transfer, the master generates the clock and the START and STOP conditions, while the receiver is responsible for acknowledging the reception. An Acknowledge (ACK) is signaled by the receiver pulling the SDA line low during the ninth SCL cycle. If the receiver leaves the SDA line high, a NACK is signaled.

The AM4096 has a default slave address of 00h. This address can be changed for each device. The functionality of the device can be programmed on the addresses between 0 and 55 with 16 bit long words.

Address	Functionality
00–31	Read/Write EEPROM
32–35	Read registers for reading the output data
40–41	Write registers for factory tests
48–55	Read / Write registers with settings

The AM4096 device acts as a slave and supports two modes:

1. Master transmits to slave. This mode is used to write to the AM4096 address space. The 16 bit data word is divided into two 8 bit data frames. The ACK acknowledges are provided by the slave.

Fig. 6: Write data packet

After the EEPROM write packet (memory address 00 h – 1 Fh) the slave device can not be addressed for a time of 20 ms. In this time the slave is performing the internal EEPROM write process. If the device is addressed, no ACK is returned.

2. Combined format mode is used to read the AM4096 address space. If the EEPROM address space is addressed (00 h – 1 Fh), then the slave uses clock stretching during the internal EEPROM read time (minimum 20 µs).

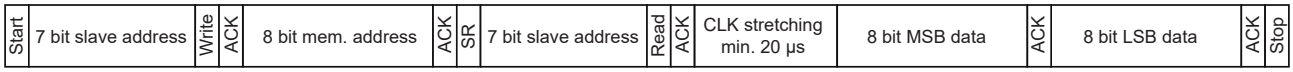


Fig. 7: EEPROM read data packet, with clock stretching

If the R or R/W registers are addressed, then the device response is immediate. After the two DATA packets the ACK is not verified.

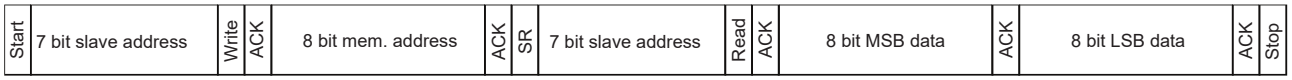


Fig. 8: Register read data packet

Memory address space

		ADR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EEPROM	R/W	0	Pdint	AGCdis	-	Slowint	Pdtr			Pdie	Reg35	-	Addr					
		1	Abridis	Bufsel		Sign	Zin											
		2	Nfil								Daa	Hist						
		3	Dact	Dac		SSIcfg		-	-	Sth		UVW			Res			
	R/W	4	Factory settings data.															
		5																
		6																
		7																
	R/W	8	Free EEPROM space															
		9																
		10																
		...																
		28																
		29																
	R/W	30	Device identification number.															
		31																
REGISTERS	R	32	SRCH	-	-	-	Rpos											
		33	SRCH	-	-	-	Apos											
		34		Weh	Wel	-												
		35	AGCgain				-	Thof	Tho									
	R/W	...	Not available															
		40	Only for testing. For normal operation must be zeros.															
		41																
	R/W	...	Not available															
		48	Pdint	AGCdis	-	Slowint	Pdtr			Pdie	Reg35	-	Addr					
		49	Abridis	Bufsel		Sign	Zin											
		50	Nfil								Daa	Hist						
		51	Dact	Dac		SSIcfg		-	-	Sth		UVW			Res			
	R/W	52	Factory settings data.															
		53																
		54																
		55																

AM4096 has EEPROM and registers with 16 bit word organization. AM4096 operates according to the contents in registers. When the chip is powered-on the EEPROM content from address 0 to 7 is copied to the registers from 48 to 55. This is also done with every change in the EEPROM. Registers from 48 to 51 can be accessed for fast non-permanent setting changes. Registers from 32 to 35 can be used for fast readings of the measured data.

Description of user-programmable parameters:

Parameter	Length	Description	Logic	Default	Note
Pdint	1	Interpolator power	0 = on, 1 = off	0	Interpolator power can be switched off, if only analogue outputs are used.
AGCdis	1	AGC disable	0 = AGC on, 1 = AGC off	0	
Slowint	1	Interpolator delay	0 = on, 1 = off	1	It must always be set to 1. Currently it is not allowed to use value 0.
Pdtr	2	Internal power down rate	00 = 1:128, 01 = 1:256, 10 = 1:512, 11 = 1:1024	11	See power save mode description.
Pdie	1	Internal power down	0 = disabled, 1 = enabled	0	See power save mode description.
Reg35	1	Regulator voltage	0 = 3 V, 1 = 3.3 V	1	
Adr	7	Device address	From 0 to 127	0	Default address is set to 0.
Abridis	1	Enabling A B Ri outputs	0 = enabled, 1 = disabled	0	Incremental output can be disabled if not used.
Bufsel	1	Selects the output on pins U/N_{Sin}, V/P_{Sin}, W/N_{Cos}, Td/P_{Cos}	0 = UVW, Tacho direction 1 =Sinusoidal differential	0	Interpolator may not work properly when sinusoidal differential analogue outputs are on.
Monsel	1	Test parameter		0	Must be zero.
Sign	1	Selects the output direction	0 = positive, 1 = negative	0	
Zin	12	Zero position data	0 = 0°, 4,095 = 360°	0	
Nfil	8	Test parameters		0	Must be zeros.
Daa	1	Output position selection	0 = relative, 1 = absolute	0	Absolute position is not affected by zeroing while relative position is.
Hist	7	Digital hysteresis value in LSB at 12 bit resolution	From 0 to 127	0	
Dact	1	Select the output on V_{out}/T_{out} pin	0 = position data on V_{out}/T_{out} pin 1 = tacho data on V_{out}/T_{out} pin	0	
Dac	2	Linear voltage period selection	00 = 360°, 01 = 180°, 10 = 90°, 11 = 45°	0	
SSIcfg	2	SSI settings		01	See SSI description.
Sth	3	Tacho measuring range		0	See table in tacho output description.
UVW	3	UVW number of periods/ turn	000 = 1, 001 = 2, 010 = 3, 011 = 4, ..., 111 = 8	0	
Res	3	Interpolation factor rate	000 = 4,096, 001 = 2,048, ... 110 = 64, 111 = 32	0	

Description of status and encoder output values:

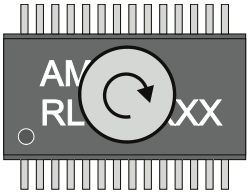
SRCH	1	Output position data valid	0 = valid data 1 = data not valid yet
Rpos	12	Relative position inf.	0 = 0°, 4,095 = 360°
Apos	12	Absolute position inf.	0 = 0°, 4,095 = 360°
Weh	1	Magnet too far status	0 = magnet distance ok, 1 = magnet is too far
Wel	1	Magnet too close status	0 = magnet distance ok, 1 = magnet is too close
Thof	1	Tacho overflow info	0 = speed in range, 1 = speed out of range
Tho	10	Tacho output data	0 = 0, 1,023 = full measuring range

3/5 V operation mode

The AM4096 can operate with power supply voltage from 3 V to 5.5 V. The outputs and inputs are supplied with the external voltage. The core of the chip is always powered with the regulated voltage from the LDO voltage regulator. The voltage of the regulator can be selected with the “Reg35” parameter between 3 V and 3.3 V. When the external power supply is from 3 V to 3.3 V the regulator voltage should be set to 3 V. When the external power supply voltage is from 3.3 V to 5.5 V the regulator voltage should be set to 3.3 V.

Outputs direction

The direction of the outputs can be changed by changing the “Sign” parameter. The arrow in picture shows clockwise (CW) rotation of the magnet. The picture is a top view of the magnet placed above the AM4096.



Sinusoidal analogue outputs for filtering

Agnd is an internally generated reference voltage. It is used as a zero level for the analogue signals, the voltage is typically 1.55 V. Pins 10 and 11 are unbuffered sinusoidal analogue outputs used for filtering and for testing purposes.

Unbuffered sinusoidal outputs:

Parameter	Symb.	Min	Typ	Max	Unit
Internal serial impedance	R_n		2		kΩ

The chart below shows the timing diagram for CW rotation of the recommended magnet.
Sinusoidal outputs produce one period of sine and cosine signal per turn with phase difference of 90°. Each signal has the same amplitude and minimum offset with respect to Agnd.
AGC controls the amplitude of the signals within 20%. AGC can be disabled if “AGCdis” parameter is set to 1.

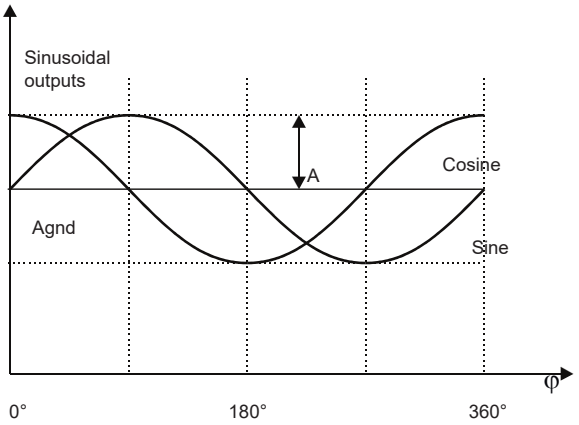


Fig. 9: Timing diagram for analogue output

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Amplitude	A	0.5	0.83	1.1	V	*
Vref voltage	V_{Vref}		1.55		V	
Max. frequency	f_{Max}		1000		Hz	

* Amplitude = 1/2 of peak to peak value.

Sinusoidal differential analogue outputs

Sinusoidal signals can be output as sinusoidal differential signals when the “BufSel” parameter is set to 1. The interpolator may not work properly when the differential analogue outputs are on. If analogue outputs are not needed then the “BufSel” parameter should be set to 0.

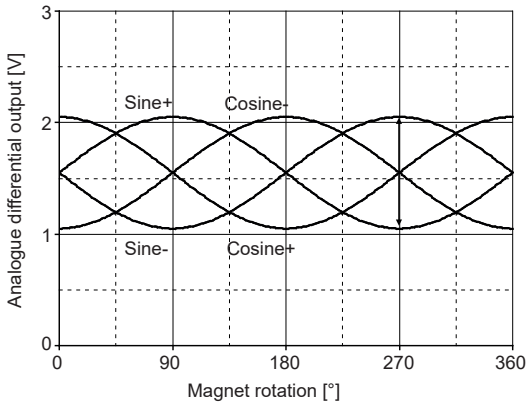


Fig. 10: Timing diagram for differential analogue output

Pin name	Pin function
“W/N_{Cos}”	Cosine negative
“V/P_{Sin}”	Sine positive
“U/N_{Sin}”	Sine negative
T_d/P_{Cos}	Cosine positive

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Amplitude	A	1	1.66	2.2	V	*
Amplitude difference	d_A		0	0.5	%	
Phase difference	d_{Ph}	89.8	90	90.2	°	
Sine offset	S_{offs}	–5	0	5	mV	
Cosine offset	C_{offs}	–5	0	5	mV	
Max. frequency	f_{Max}		1000		Hz	

* Amplitude = 1/2 of peak to peak value of the difference between the positive and negative signal.
The distance to the magnet and the temperature are within tolerances. To prevent saturation of the signals, the amplitude must never exceed 2.2 V.

AGC

Automatic gain control is enabled when the “AGCdis” parameter is set to 0. If the magnetic signal is changing the AGC is able to control the output signal amplitude in range between 0.8 V and 1 V. When the amplitude is less than 0.8 V, the gain is increased. When the amplitude is more than 1 V, the gain is decreased. The AGC gain has 16 levels and the range is from 0.5 to 2. Level 8 is at normal magnetic conditions.

Interpolator

When the magnet is rotated for 360° the sensors generates two perfect sinusoidal signals with phase difference of 90°. The interpolator is using those sinusoidal signals to calculate the current angle position and the angle position is output in various output formats. The calculation is performed in less than 1µs. The interpolation rates is selectable from 64 to 4096.

“Res” value	Interpolation rate	Resolution	Max. input freq.
0 0 0	4,096	0.0879°	500 Hz
0 0 1	2,048	0.1758°	1000 Hz
0 1 0	1,024	0.3516°	1000 Hz
0 1 1	512	0.7031°	1000 Hz
1 0 0	256	1.4062°	1000 Hz
1 0 1	128	2.8125°	1000 Hz
1 1 0	64	5.625°	1000 Hz
1 1 1	32	11.25°	1000 Hz

Zeroing

The output angle position data can be zeroed at any angle with resolution of 0.0879°. The relative output position is a difference between absolute position and data in zero register. The value in zero register can be changed by writing a desired value with TWI interface or with using a “Zero” input pin. With low to high transition of a signal on “Zero” pin the current absolute value is stored in zero register. When zeroing the relative position the chip must not be in power-save mode as the EEPROM is not accessible.

Incremental output

There are three signals for the incremental output: A, B and Ri. Signals A and B are quadrature signals, shifted by 90°, and signal Ri is a reference mark. The reference mark signal is produced once per revolution. The width of the Ri pulse is 1/4 of the quadrature signal period and it is synchronized with the A and B signals. The position of the reference mark is at zero.

The chart below shows the timing diagram of A, B and Ri signals with CW rotation of the magnet and positive counting direction. B leads A for CW rotation. The counting direction can be changed by programming the EEPROM with the “Sign” parameter.

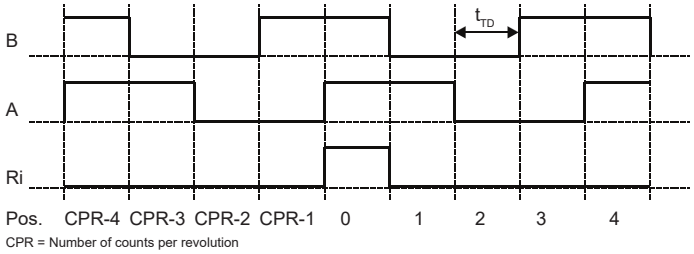


Fig. 11: Timing diagram for incremental output

The transition distance (t_{TD}) is the time between two output position changes. The transition distance time is limited by the interpolator and the limitation is dependent on the output resolution. The counter must be able to detect the minimum transition distance to avoid missing pulses.

Binary synchronous serial output SSI

Serial output data is available in up to 12 bit natural binary code through the SSI protocol. With positive counting direction and the CW magnet rotation, the value of the output data increases.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Clock period	t_{CL}	0.25		2 × tm	µs	
Clock high	t_{CHI}	0.1		tm	µs	
Clock low	t_{CLO}	0.1		tm	µs	
Monoflop time	t_m	15	19	25	µs	

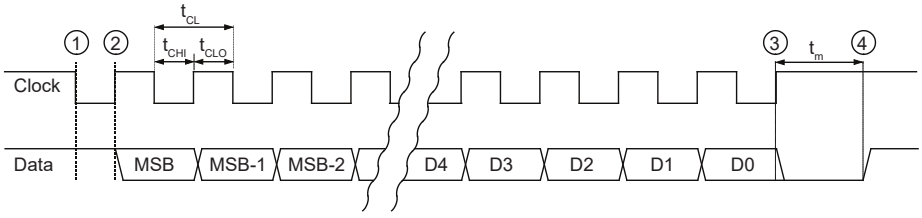


Fig. 12: SSI timing diagram with monoflop timeout

The controller interrogates the AM4096 for its positional value by sending a pulse train to the Clock input. The Clock signal must always start from high. The first high/low transition (point 1) stores the current position data in a parallel/serial converter and the monoflop is triggered. With each transition of Clock signal (high/low or low/high) the monoflop is retriggered. At the first low/high transition (point 2) the most significant bit (MSB) of the binary code is transmitted through the Data pin to the controller. At each subsequent low/high transition of the Clock the next bit is transmitted to the controller. While reading the data the t_{CHI} and t_{CLO} must be less than t_{mMin} to keep the monoflop set. After the least significant bit (LSB) is output (point 3) the Data goes to low. The controller must wait longer than t_{mMax} before it can read updated position data. At this point the monoflop time expires and the Data output goes to high (point 4).

SSIcfg	Descripion
0 0	No ring register operation
0 1	Ring register operation data length according to the resolution, data is not refreshed
1 0	No ring register operation
1 1	Ring register operation data length according to the resolution, data is refreshed

If the number of clocks is more than the data length than the behaviour of the SSI can be as defined with the SSIcfg parameter. If the “SSIcfg” parameter is set to 00 or 10 then the data is output only once (chart below).

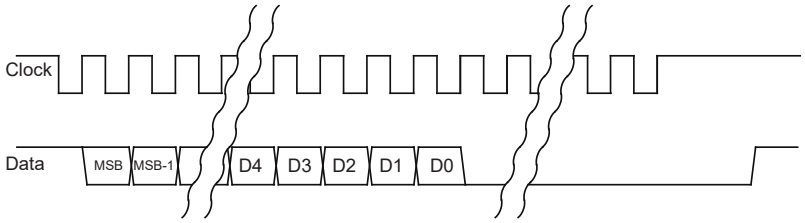


Fig. 13: SSI single read, SSIcfg is set to 00 or 10

To enlarge the reliability of reading the controller can read the same data more than once. The “SSIcfg” parameter must be set to “01” and the controller must continue sending the Clock pulses after the data is read without waiting for Tm (chart below). The same data will be output again and between the two outputs one logic zero will be output. The length of the data is depended of the resolution settings.

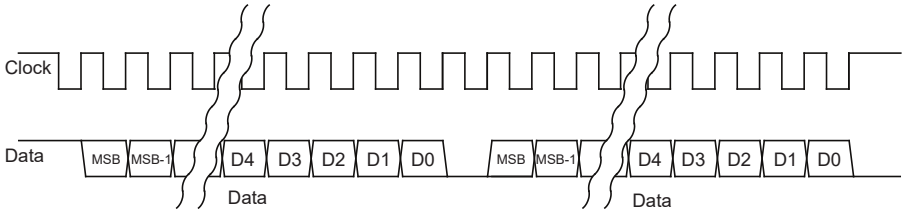


Fig. 14: SSI multi-read of the same position data, “SSIcfg” is set to 01

To speed-up the position reading of AM4096 the controller can constantly read the data. The “SSIcfg” parameter must be set to “11” and the controller must continue sending the Clock pulses after the data is read without waiting for Tm (chart below). Each data will be output as fresh position information and between the two outputs one logic zero will be output. The length of the data is depended of the resolution settings.

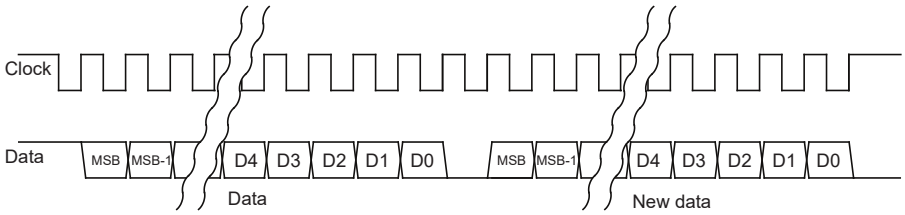


Fig. 15: SSI fast position read, SSIcfg is set to 11